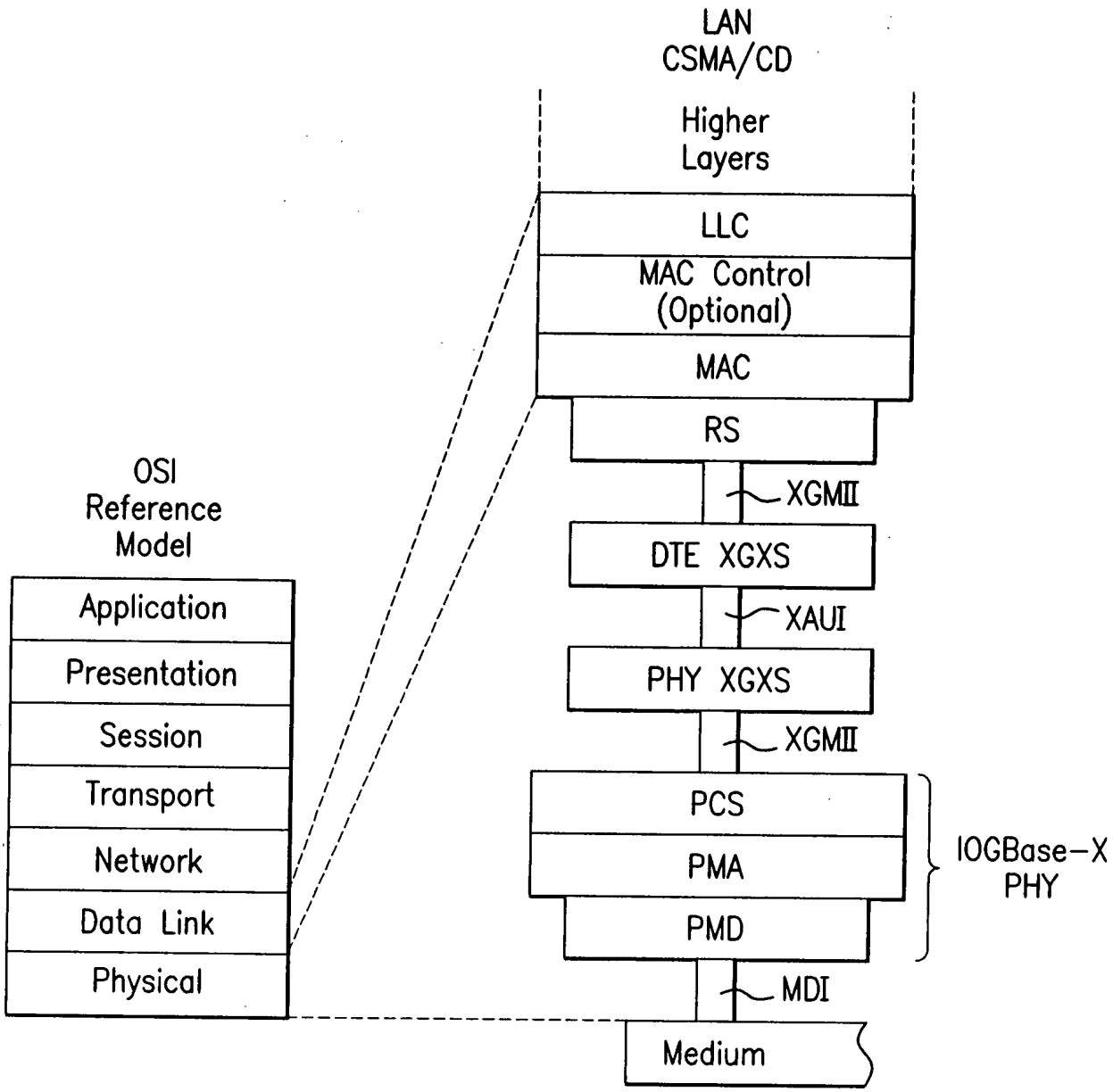

FIG. 1

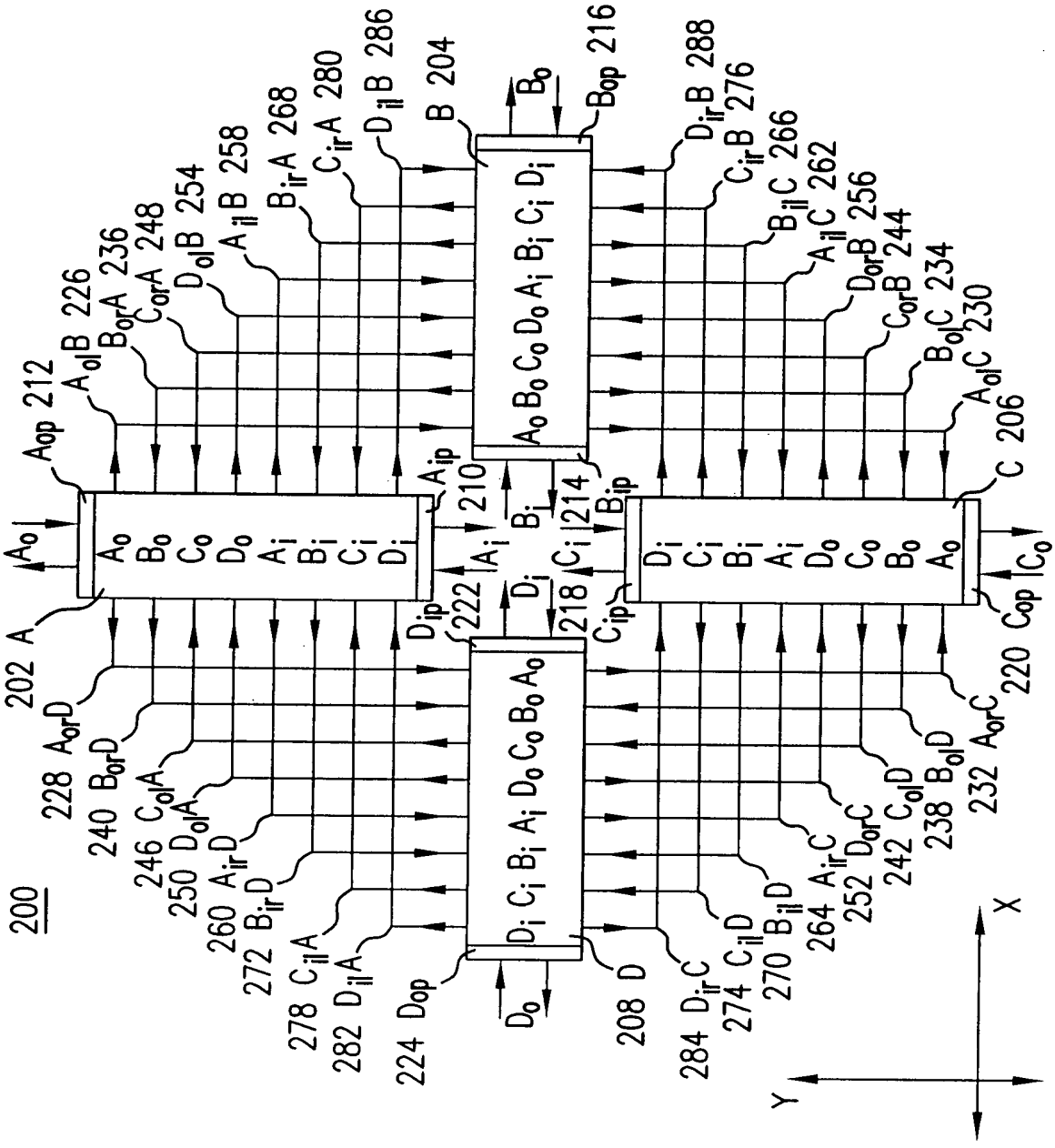
200
202 A
Aop 212
Aol B 226
Bor A 236
Cor A 248
Dol B 254
Ail B 258
Bir A 268
Cir A 280
Dil B 286
B 204
Bop 216
Dir B 288
Cir B 276
Bil C 266
Ail C 262
Dor B 256
Cor B 244
Bol C 234
Aol C 230
C 206
Aor D 228
Bor D 240
Col A 246
Dol A 250
Air D 260
Bir D 272
Cil A 278
Dil A 282
Dop 224
Aor C 232
Bol D 238
Col D 242
Dor C 252
Air C 264
Bil D 270
Cil D 274
Dir C 284
D 208
Ao
Bo
Co
Do
Ai
Bi
Ci
Di
Aip 210
Bip 214
Cip 218
Dip 222
Aop 220
X
Y

FIG. 2

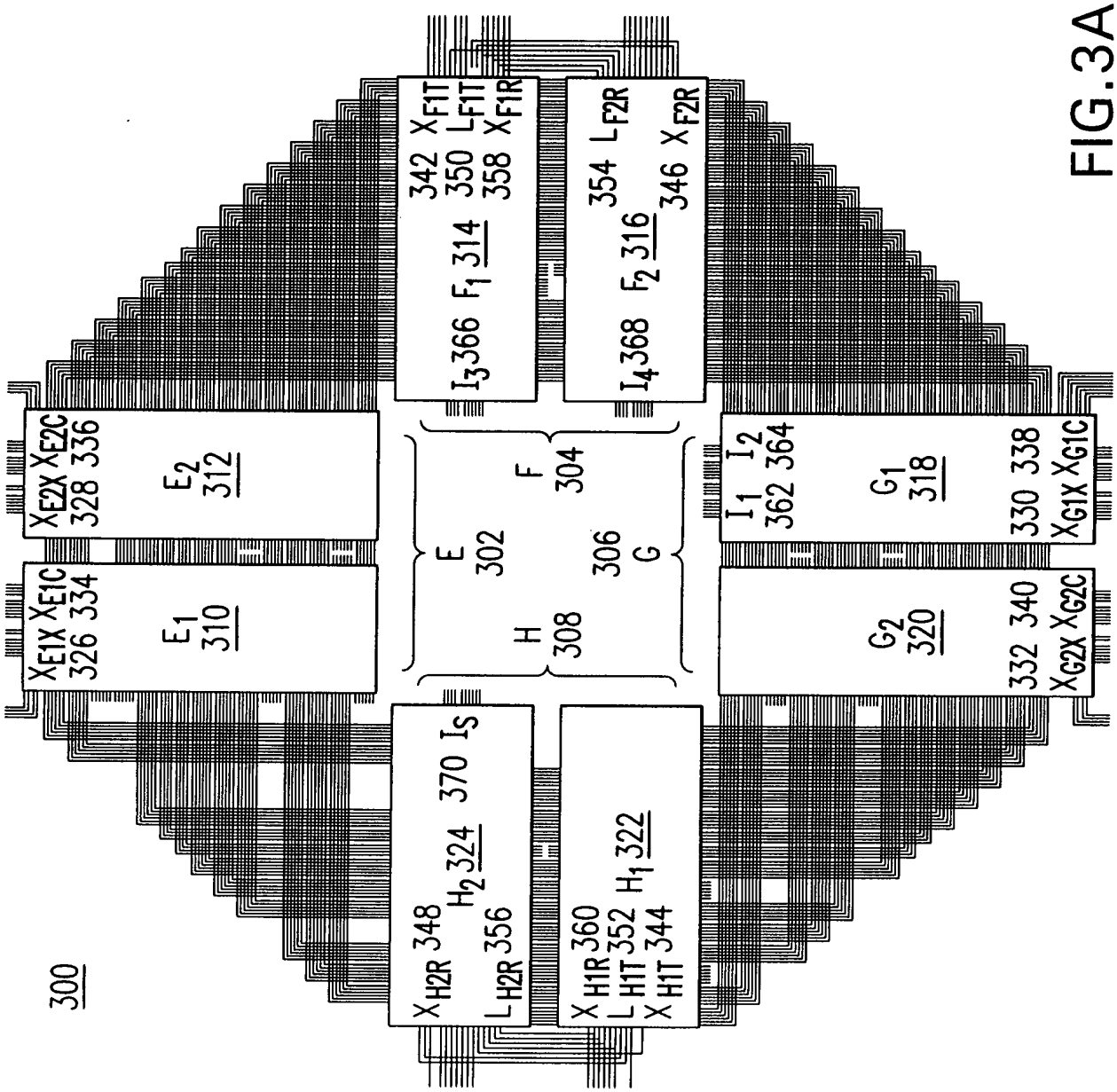
300
X_{H2R} 348
H_2 324
370 I_S
L_{H2R} 356
X_{H1R} 360
L_{H1T} 352
H_1 322
X_{H1T} 344
H 308
E 302
F 304
G 306
X_{E1X} X_{E1C} 326 334
E_1 310
X_{E2X} X_{E2C} 328 336
E_2 312
342 X_{F1T}
350 L_{F1T}
358 X_{F1R}
I_3 366 F_1 314
354 L_{F2R}
346 X_{F2R}
I_4 368 F_2 316
I_1 I_2 362 364
G_1 318
330 338 X_{G1X} X_{G1C}
G_2 320
332 340 X_{G2X} X_{G2C}

FIG. 3A

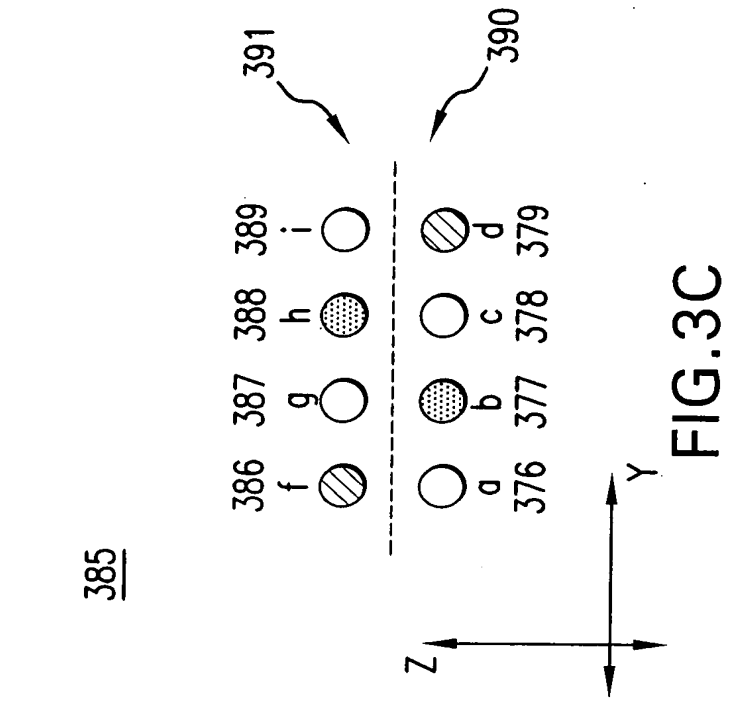
385
391
390
386 f
387 g
388 h
389 i
a 376
b 377
c 378
d 379
Z
Y

FIG.3C

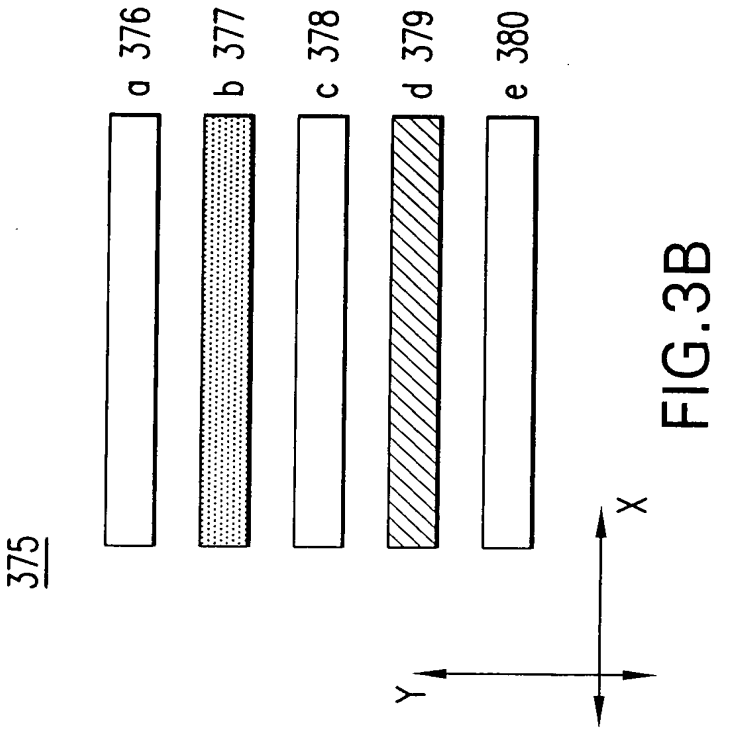
375
a 376
b 377
c 378
d 379
e 380
Y
X

FIG.3B

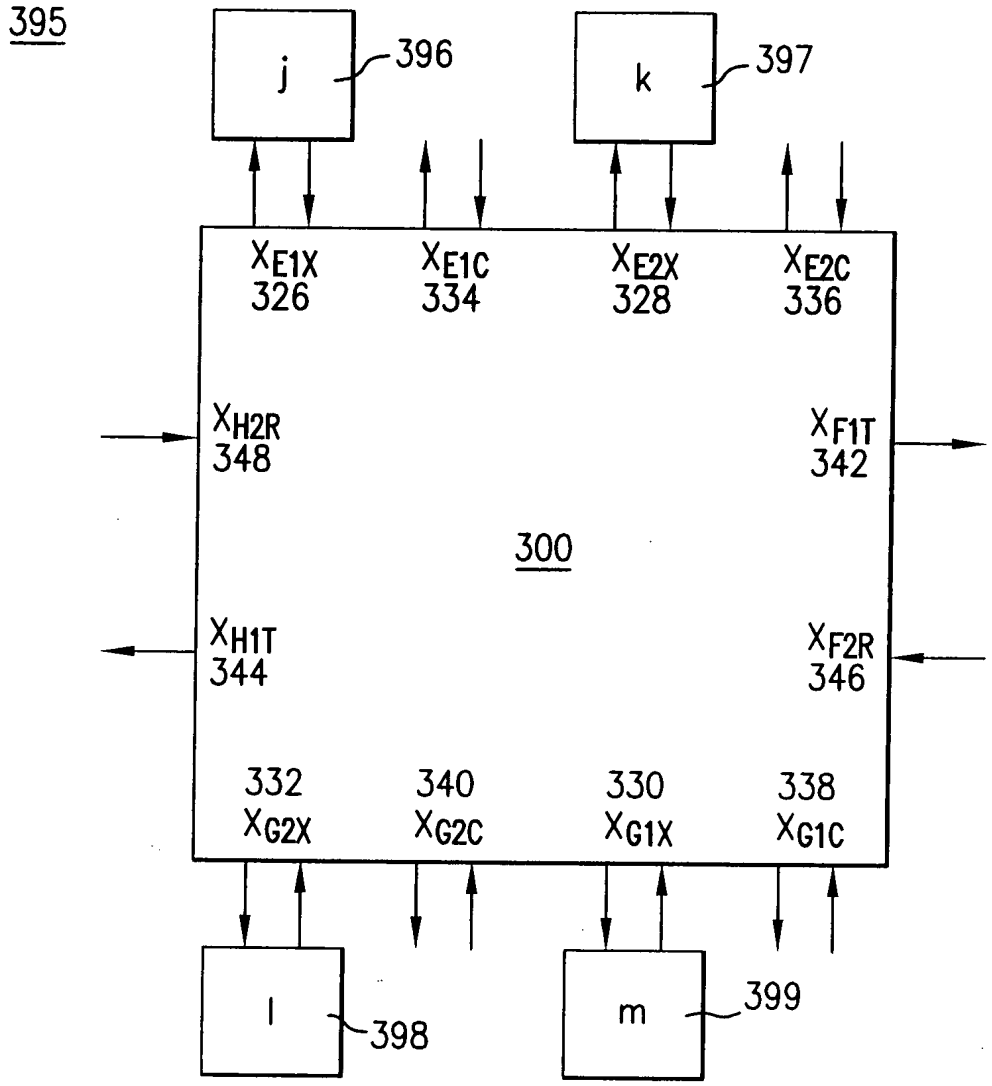
395
j
396
k
397
X_{E1X} 326
X_{E1C} 334
X_{E2X} 328
X_{E2C} 336
X_{H2R} 348
X_{F1T} 342
300
X_{H1T} 344
X_{F2R} 346
332 X_{G2X}
340 X_{G2C}
330 X_{G1X}
338 X_{G1C}
l
398
m
399

FIG.3D

TABLE 400

XAUI Protocol		
Received From Out of Bus	Communicated Within Bus	Transmitted to Out of Bus
40 data bits	40 data bits	80 data bits
4 link bits	4 link bits	
4 lock bits	4 lock bits	
4 clock bits	4 clock bits	4 clock bits
4 fast clock bits	4 fast clock bits	
1 CLOCK MODE SELECT bit	1 CLOCK MODE SELECT bit	

CDL Protocol		
Received From Out of Bus	Communicated Within Bus	Transmitted to Out of Bus
40 data bits	40 data bits	80 data bits
4 link bits	4 link bits	4 link bits
4 lock bits	4 lock bits	4 lock bits
4 clock bits	4 clock bits	4 clock bits
4 fast clock bits	4 fast clock bits	
1 CLOCK MODE SELECT bit	1 CLOCK MODE SELECT bit	

XGMII Protocol		
Received From Out of Bus	Communicated Within Bus	Transmitted to Out of Bus
40 data bits	80 data bits	40 data bits
4 lock bits	4 lock bits	
4 clock bits	4 clock bits	4 clock bits
3 MODE SELECT bits		
1 DIFFERENTIAL CLOCK MODE SELECT bit		
	1 CLOCK MODE SELECT bit	
		4 output enable bits

FIG.4

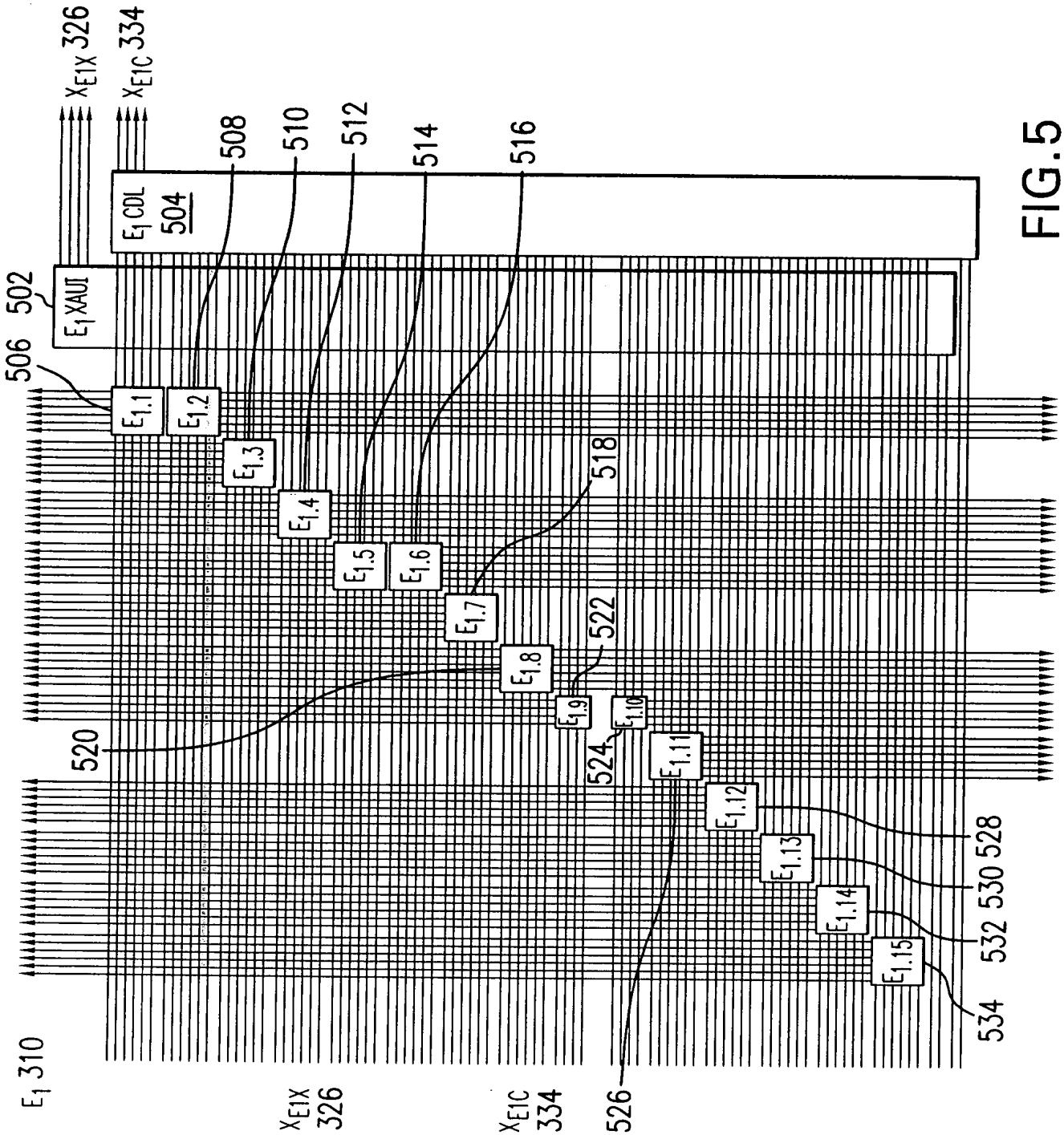
X_{E1X} 326
X_{E1C} 334
508
510
512
514
516
E_1 CDL 504
E_1 XAUI 502
506
$E_{1.1}$
$E_{1.2}$
$E_{1.3}$
$E_{1.4}$
$E_{1.5}$
$E_{1.6}$
$E_{1.7}$
$E_{1.8}$
$E_{1.9}$
$E_{1.10}$
$E_{1.11}$
$E_{1.12}$
$E_{1.13}$
$E_{1.14}$
$E_{1.15}$
518
520
522
524
526
528
530
532
534
E_1 310
X_{E1X} 326
X_{E1C} 334

FIG.5

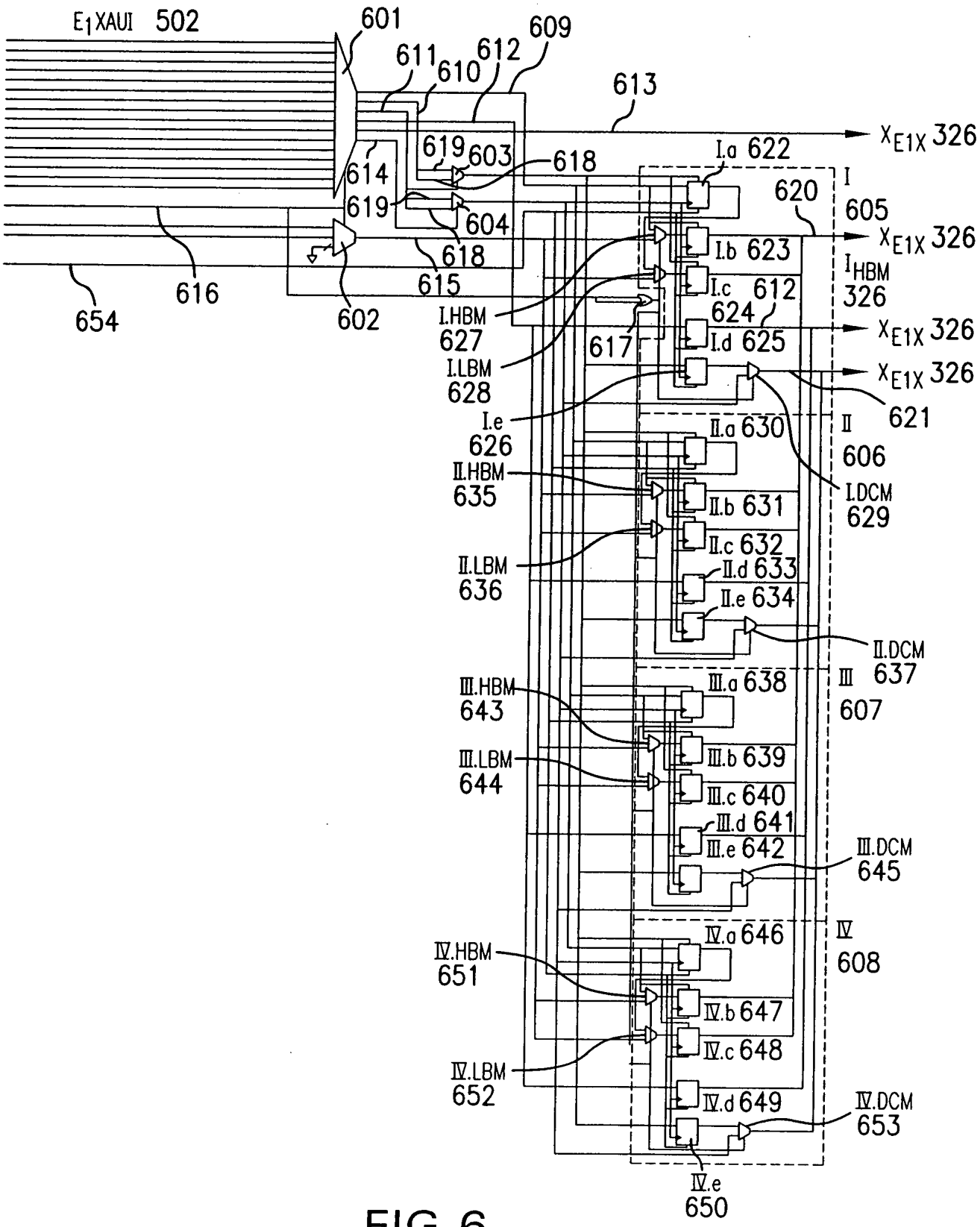
E1XAUI 502
601
611
610
612
609
613
614
619
603
618
619
604
618
615
616
654
602
617
I.a 622
620
I 605
I.b 623
I.c 612
624
I.d 625
I.e 626
I.HBM 627
I.LBM 628
I.DCM 629
621
II.a 630
II 606
II.HBM 635
II.b 631
II.c 632
II.d 633
II.e 634
II.LBM 636
II.DCM 637
III.a 638
III 607
III.HBM 643
III.b 639
III.c 640
III.d 641
III.e 642
III.LBM 644
III.DCM 645
IV.a 646
IV 608
IV.HBM 651
IV.b 647
IV.c 648
IV.LBM 652
IV.d 649
IV.DCM 653
IV.e 650
XE1X 326
IHBM 326

FIG.6

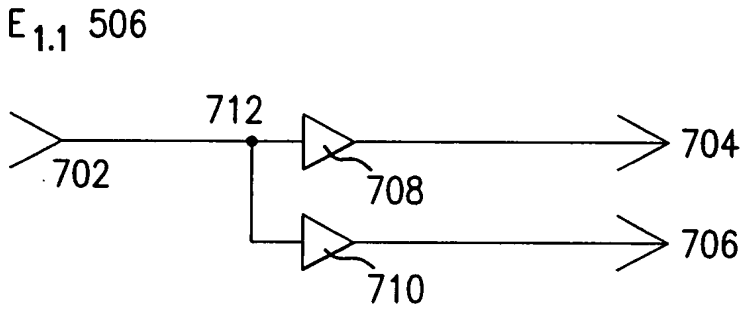
$E_{1.1}$ 506
712
702
704
708
706
710

FIG. 7

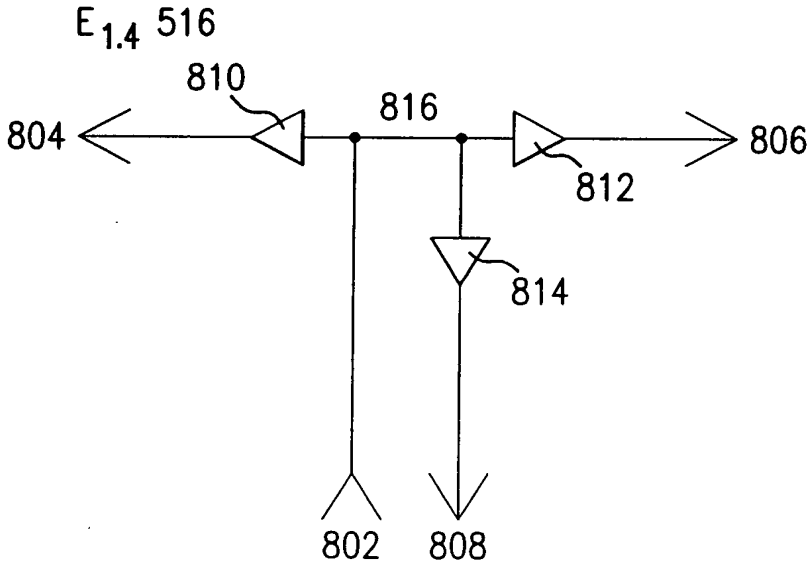
$E_{1.4}$ 516
810
816
804
806
812
814
802
808

FIG. 8

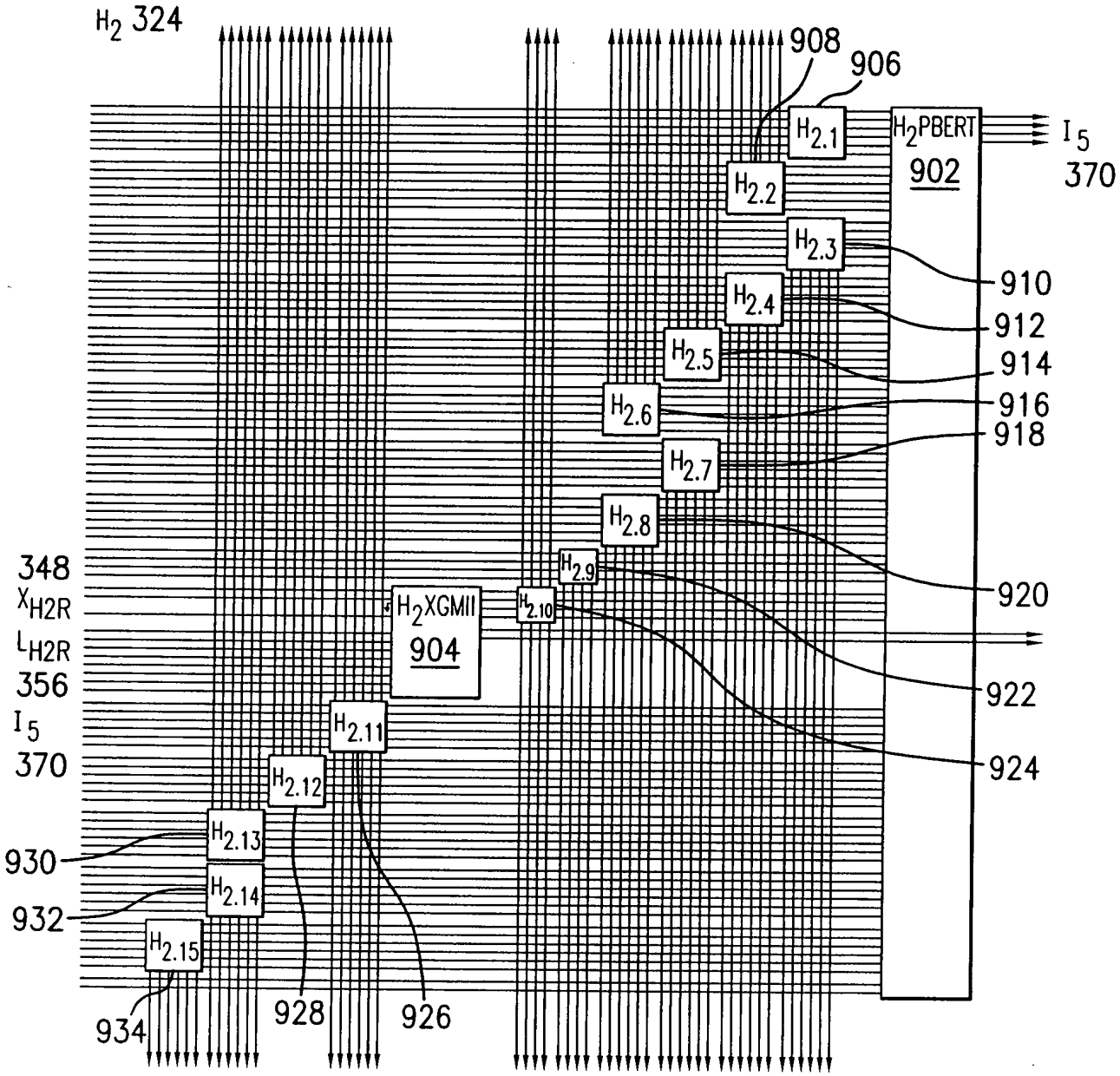
H2 324
908
906
H2.1
H2PBERT
902
I5
370
H2.2
H2.3
910
H2.4
912
H2.5
914
H2.6
916
H2.7
918
H2.8
920
H2.9
H2.10
H2XGMII
904
348
XH2R
LH2R
356
I5
370
H2.11
922
H2.12
924
H2.13
930
H2.14
932
H2.15
934
928
926

FIG.9

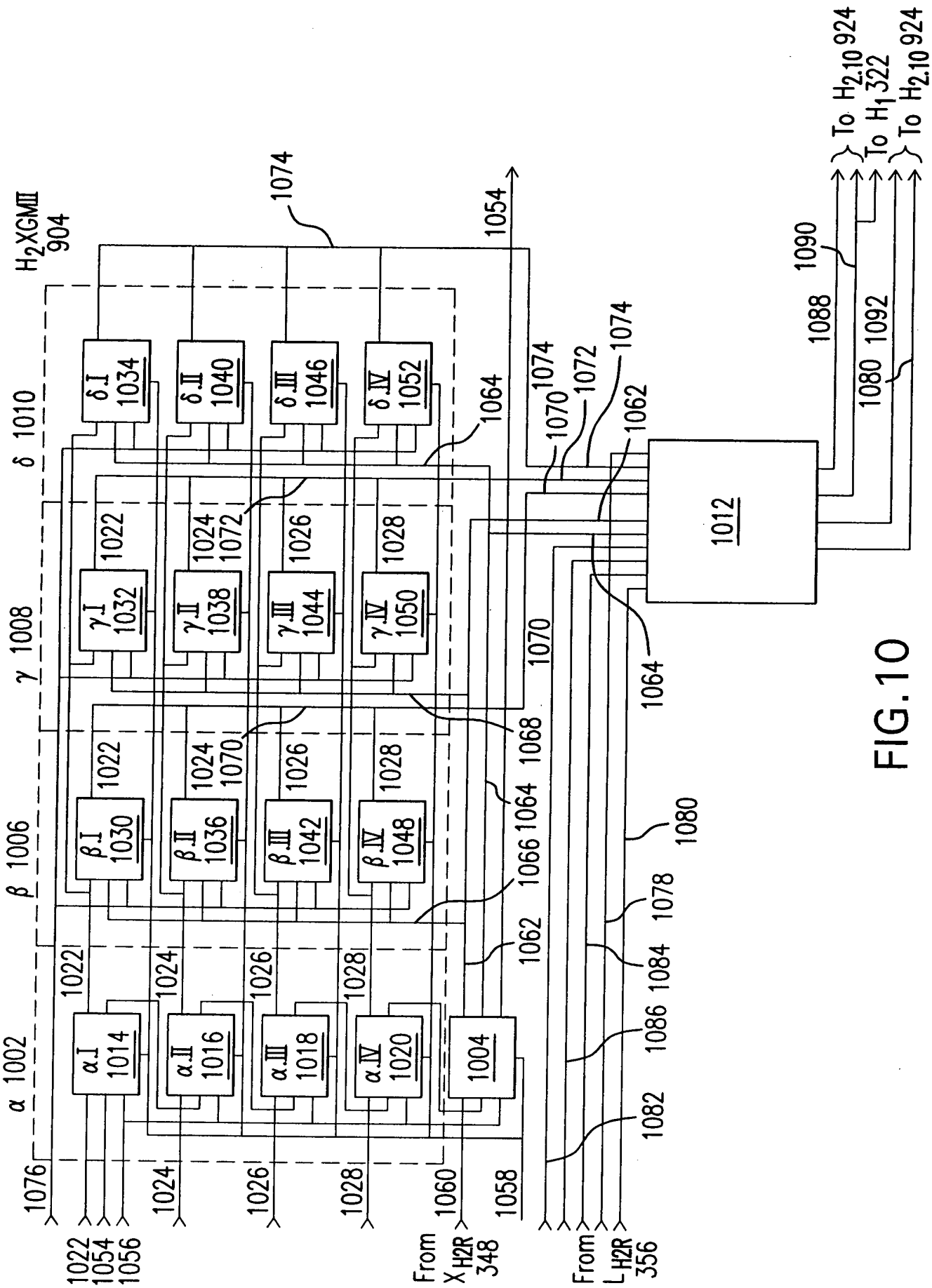
H2XGMII 904
α 1002
β 1006
γ 1008
δ 1010
αI 1014
αII 1016
αIII 1018
αIV 1020
βI 1030
βII 1036
βIII 1042
βIV 1048
γI 1032
γII 1038
γIII 1044
γIV 1050
δI 1034
δII 1040
δIII 1046
δIV 1052
1004
1012
1022
1024
1026
1028
1054
1056
1058
1060
1062
1064
1066
1068
1070
1072
1074
1076
1078
1080
1082
1084
1086
1088
1090
1092
From XH2R 348
From LH2R 356
To H2.10 924
To H1 322
To H2.10 924

FIG. 10

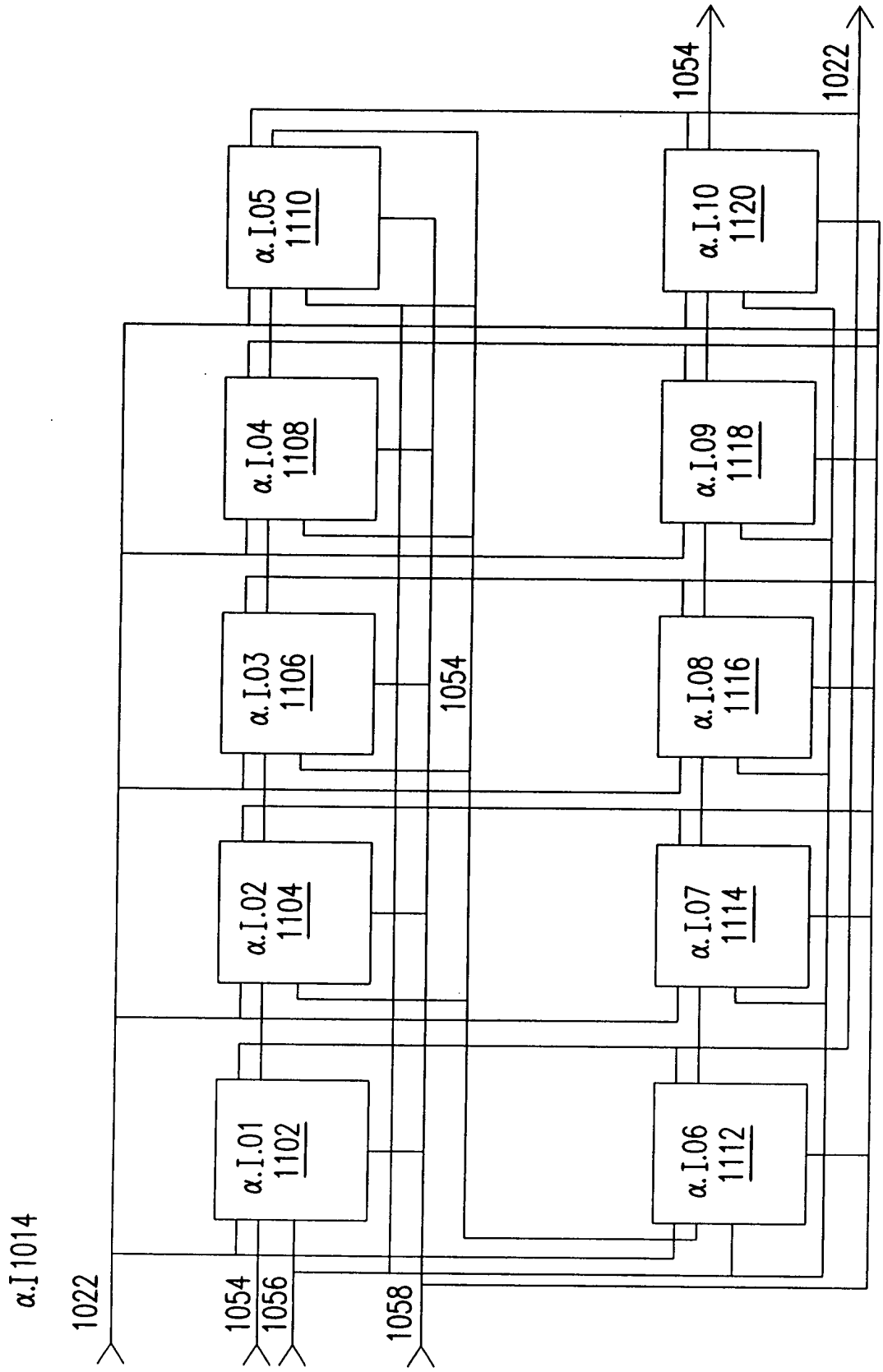
α.I1014
1022
1054
1056
1058
1054
1022
α.I.01 1102
α.I.02 1104
α.I.03 1106
α.I.04 1108
α.I.05 1110
α.I.06 1112
α.I.07 1114
α.I.08 1116
α.I.09 1118
α.I.10 1120

FIG. 11

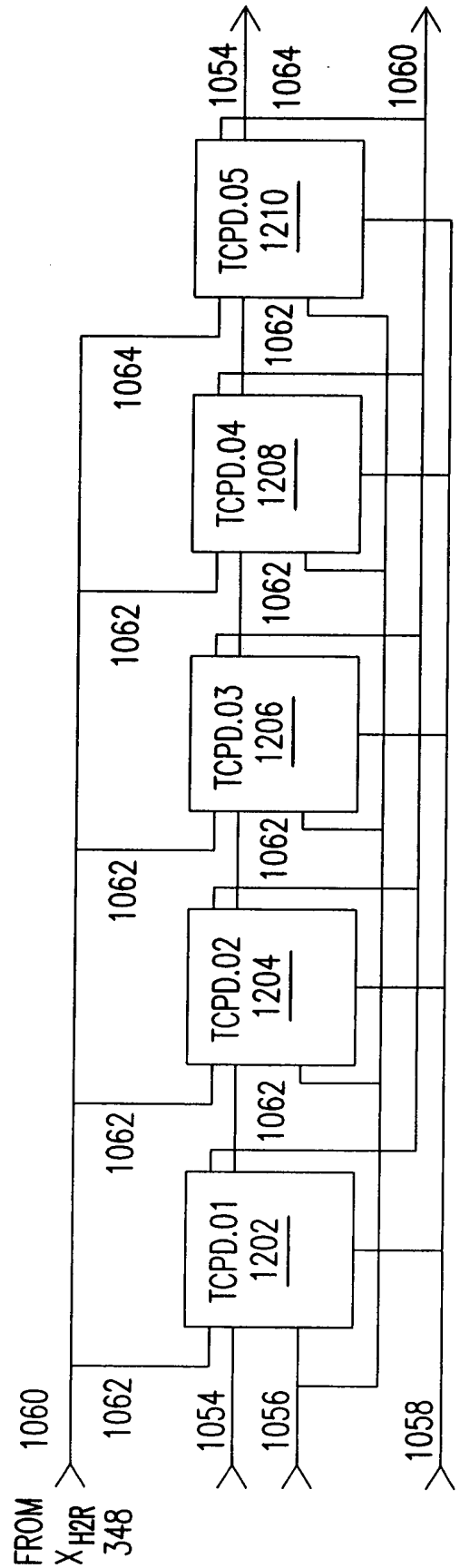
TRANSMITTER CLOCK PAD DELAY CIRCUIT 1004
FROM X H2R 348
1060
1062
1054
1056
1058
TCPD.01 1202
TCPD.02 1204
TCPD.03 1206
TCPD.04 1208
TCPD.05 1210
1062
1064
1060

FIG. 12

1380

N_9	N_{10}	N_{11}	Output
0	0	0	N_1
0	0	1	N_2
0	1	0	N_3
0	1	1	N_4
1	0	0	N_5
1	0	1	N_6
1	1	0	N_7
1	1	1	N_8

FIG.13B

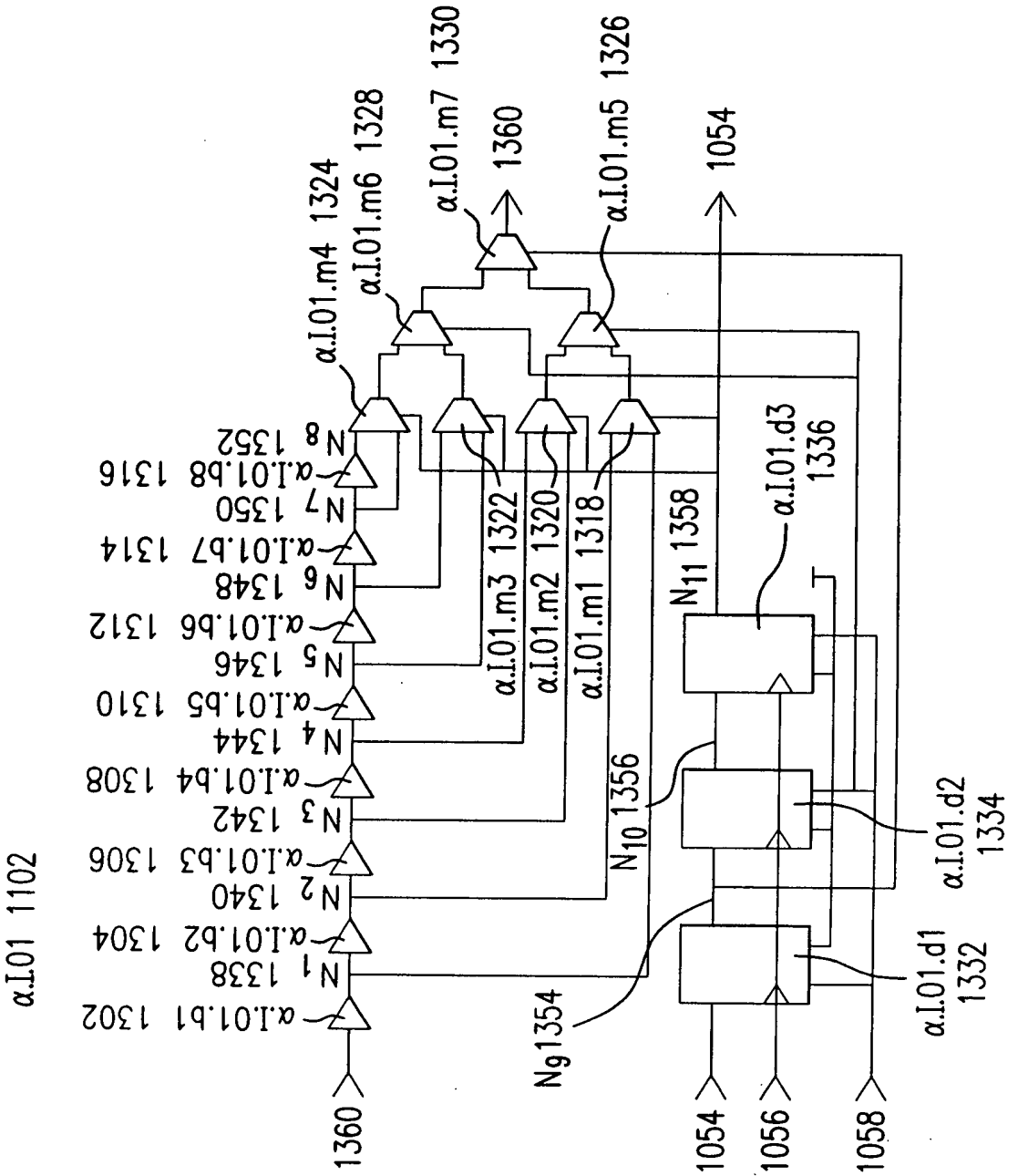

FIG.13A

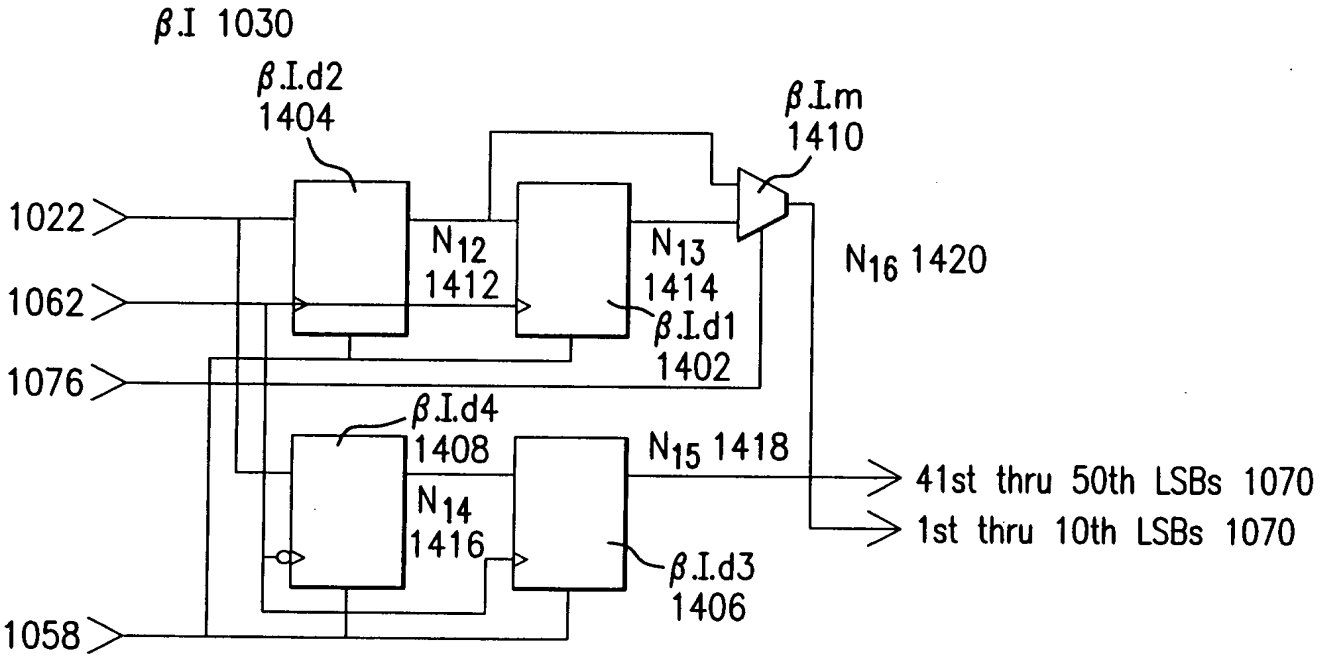
β.I 1030
β.I.d2
1404
β.I.m
1410
1022
1062
1076
1058
N12
1412
N13
1414
β.I.d1
1402
N16 1420
β.I.d4
1408
N14
1416
N15 1418
β.I.d3
1406
41st thru 50th LSBs 1070
1st thru 10th LSBs 1070

FIG. 14

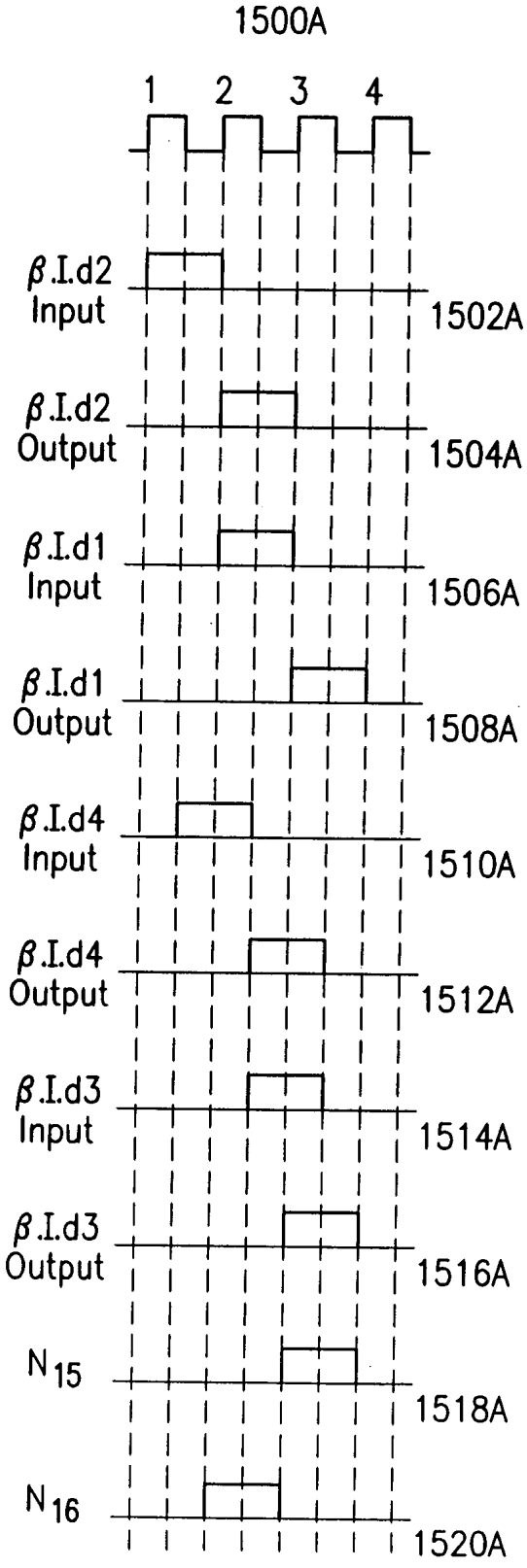

FIG.15A

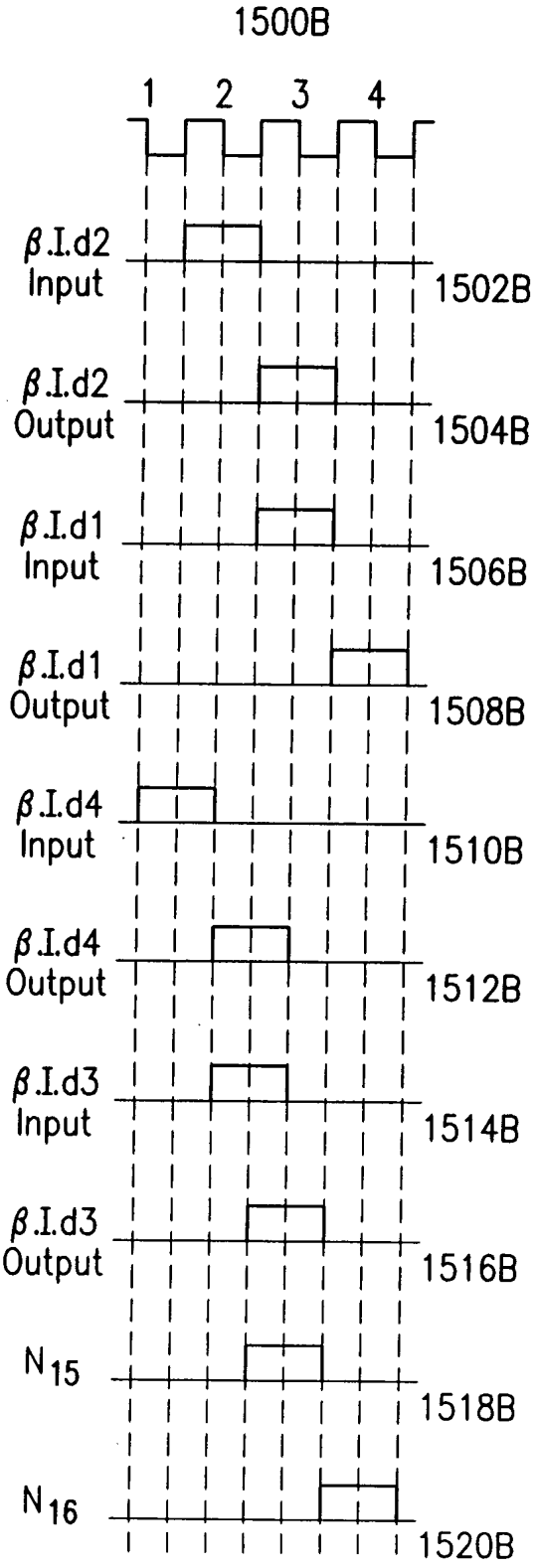

FIG.15B

TRANSMITTER REGISTER MULTIPLEXER 1012

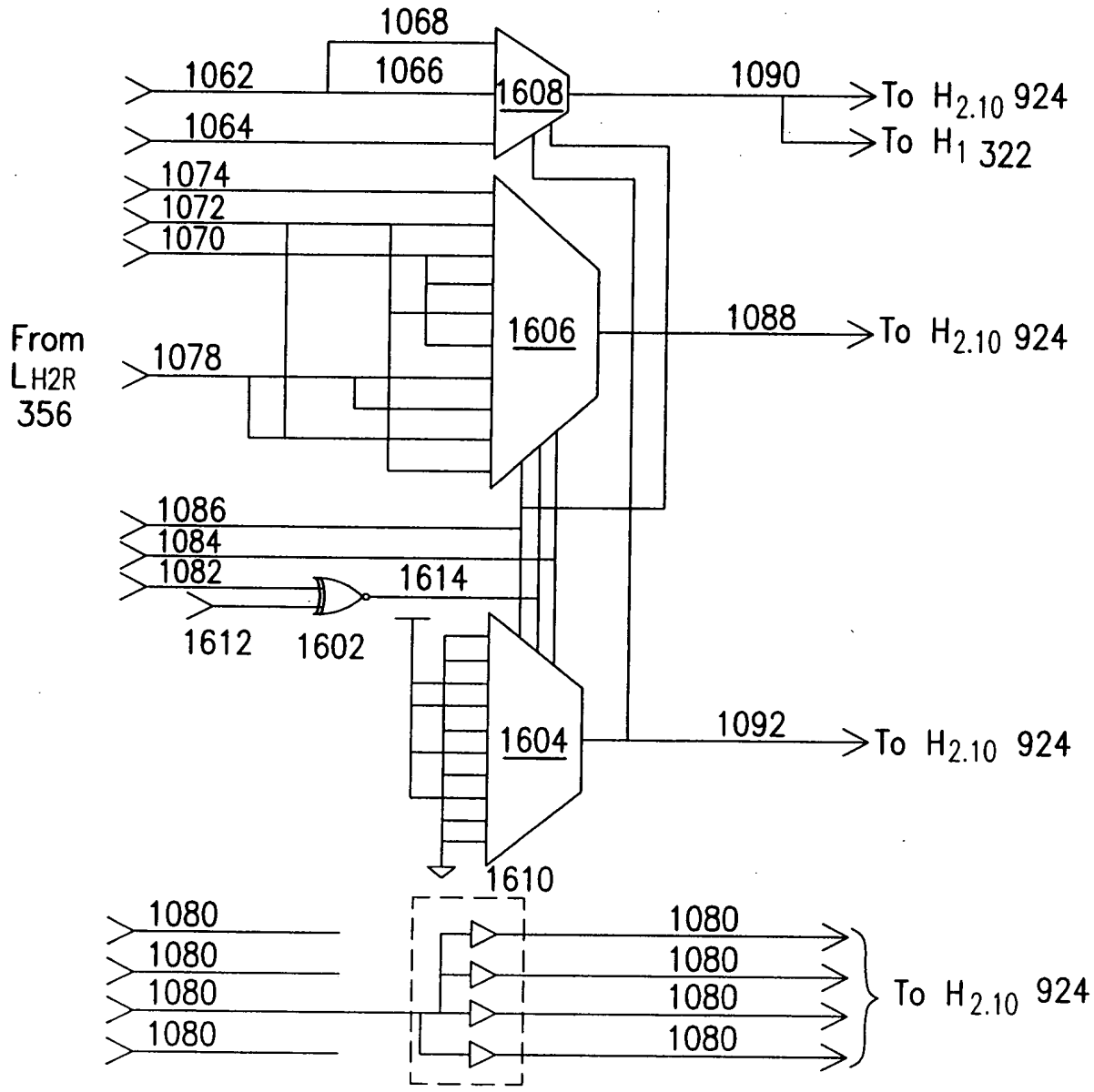

FIG. 16

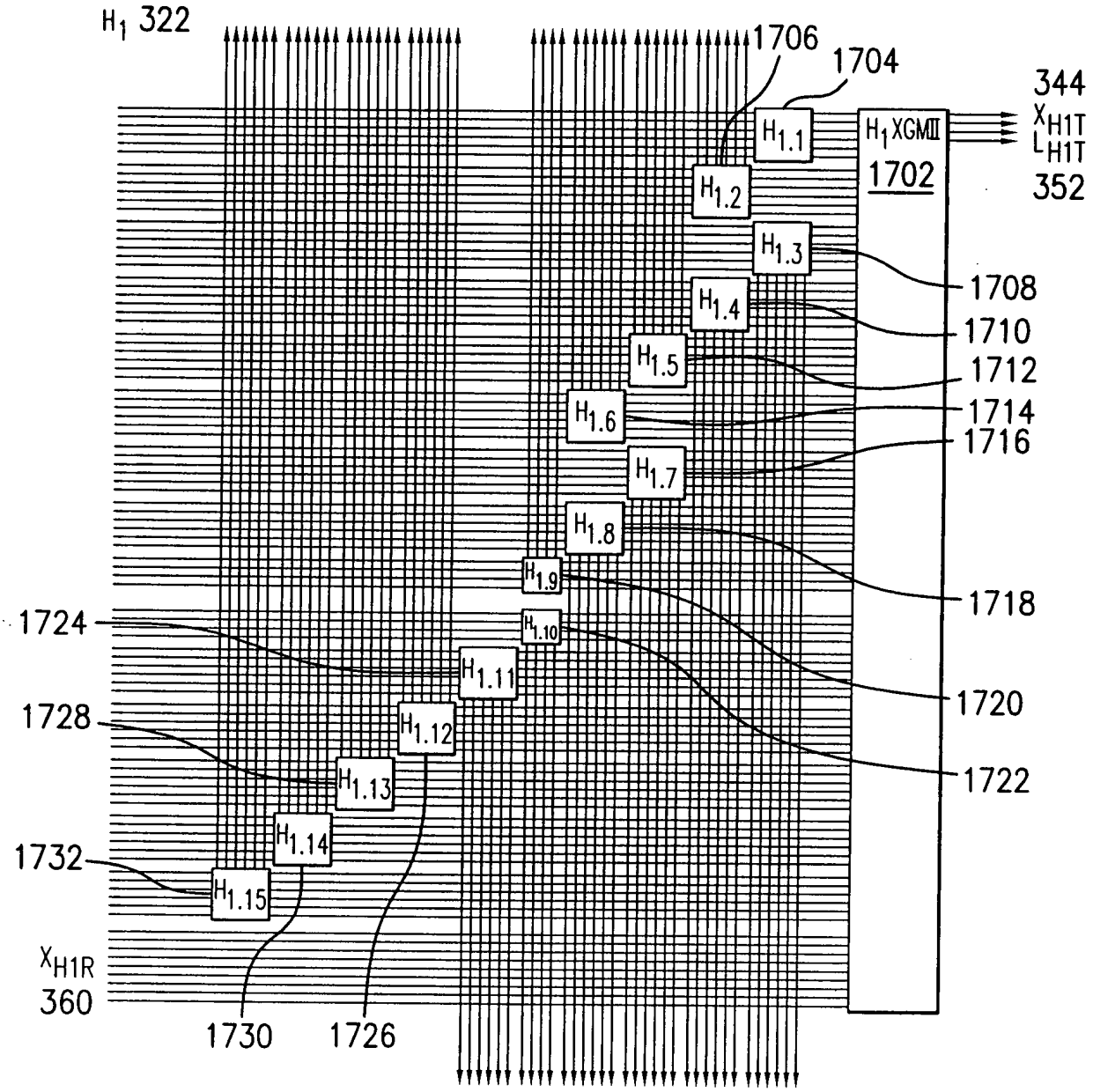
H1 322
1706
1704
344
XH1T
LH1T
352
H1.1
H1XGMII
1702
H1.2
H1.3
1708
H1.4
1710
H1.5
1712
H1.6
1714
1716
H1.7
H1.8
1718
H1.9
1724
H1.10
H1.11
1720
1728
H1.12
H1.13
1722
H1.14
1732
H1.15
XH1R
360
1730
1726

FIG. 17

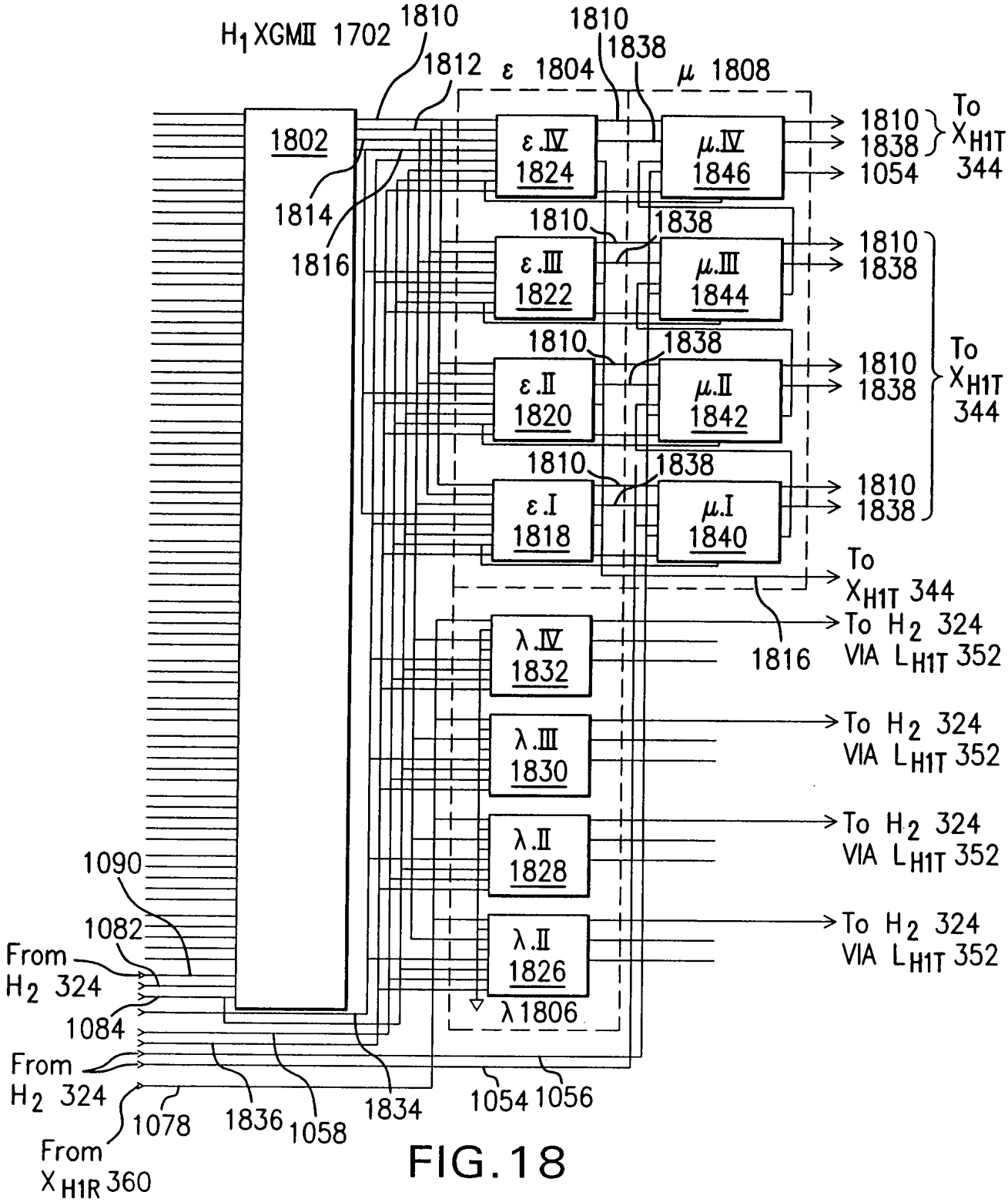
H1 XGMII 1702
1810
1812
1810
1838
ε 1804
μ 1808
1802
ε.IV 1824
μ.IV 1846
1810
1838
1054
To XH1T 344
1814
1816
1810
1838
ε.III 1822
μ.III 1844
1810
1838
1810
1838
ε.II 1820
μ.II 1842
1810
1838
To XH1T 344
1810
1838
ε.I 1818
μ.I 1840
To XH1T 344
To H2 324 VIA LH1T 352
1816
λ.IV 1832
λ.III 1830
λ.II 1828
λ.II 1826
λ 1806
To H2 324 VIA LH1T 352
To H2 324 VIA LH1T 352
To H2 324 VIA LH1T 352
1090
1082
From H2 324
1084
From H2 324
From XH1R 360
1078
1836
1058
1834
1054
1056

FIG. 18

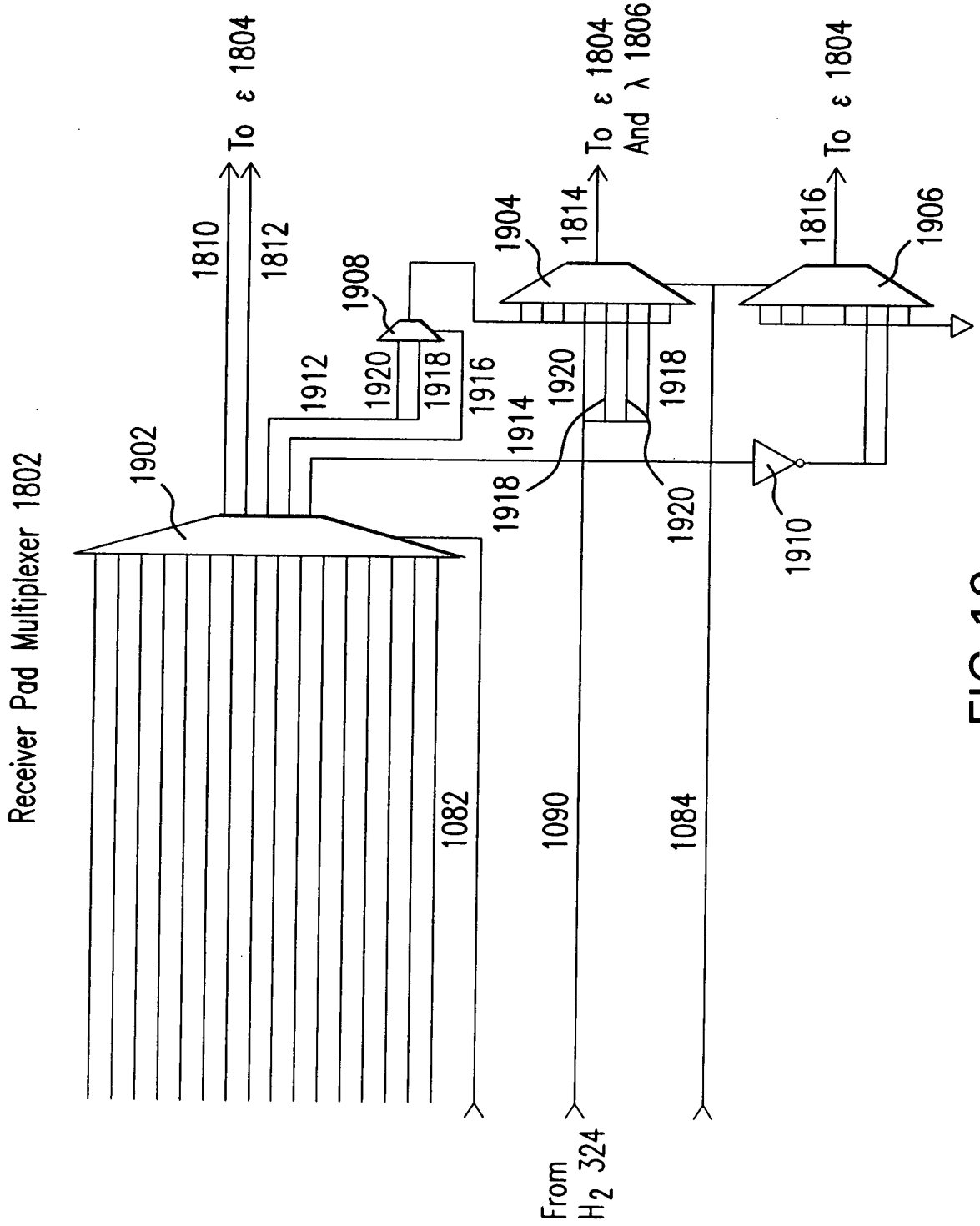
Receiver Pad Multiplexer 1802
1902
1810
To ε 1804
1812
1908
1912
1920
1918
1916
1914
1904
1814
To ε 1804
And λ 1806
1816
To ε 1804
1906
1910
1082
1090
1084
From
H_2 324

FIG. 19

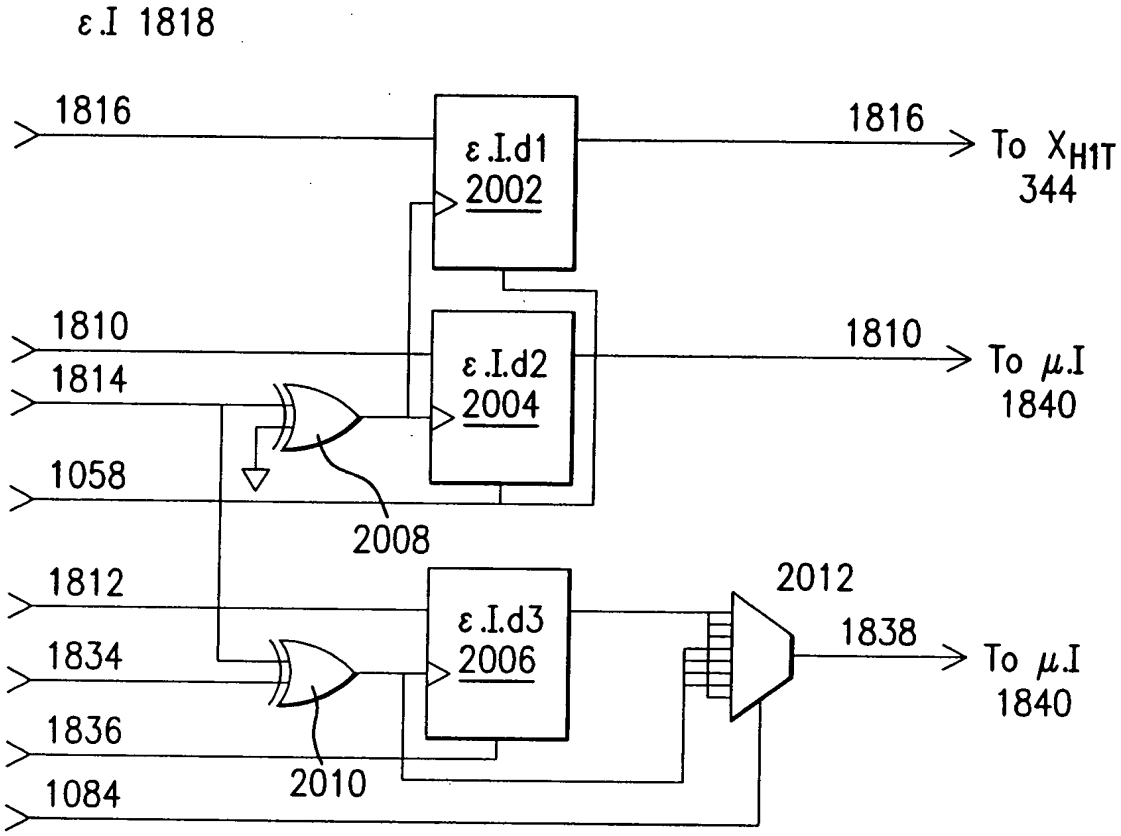
ε.I 1818
1816
ε.I.d1
2002
1816
To X_{H1T}
344
1810
1814
1058
ε.I.d2
2004
1810
To μ.I
1840
2008
1812
1834
1836
1084
ε.I.d3
2006
2010
2012
1838
To μ.I
1840

FIG.20

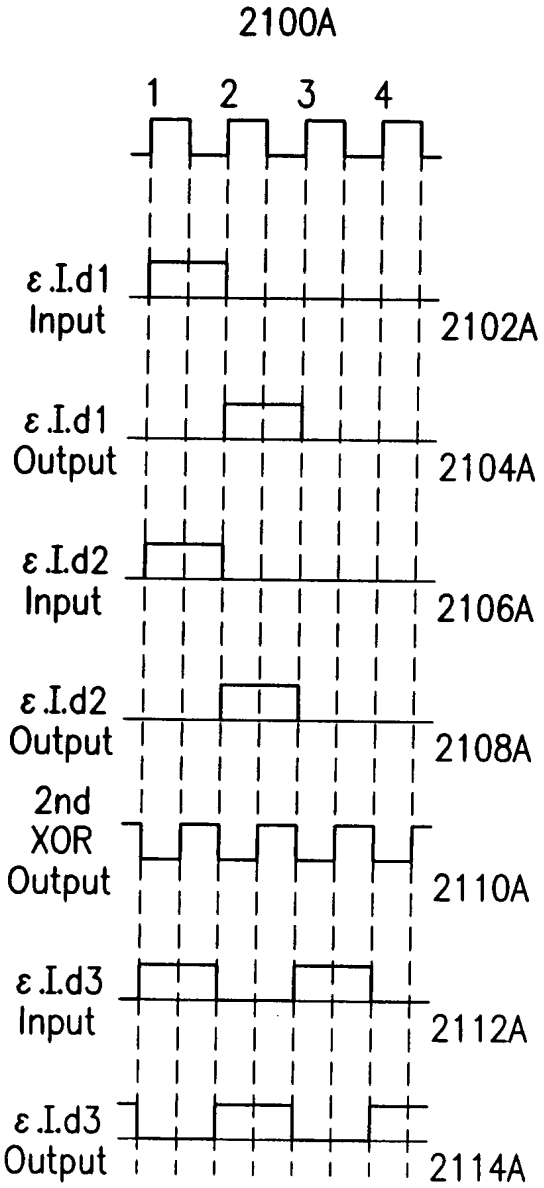

FIG.21A

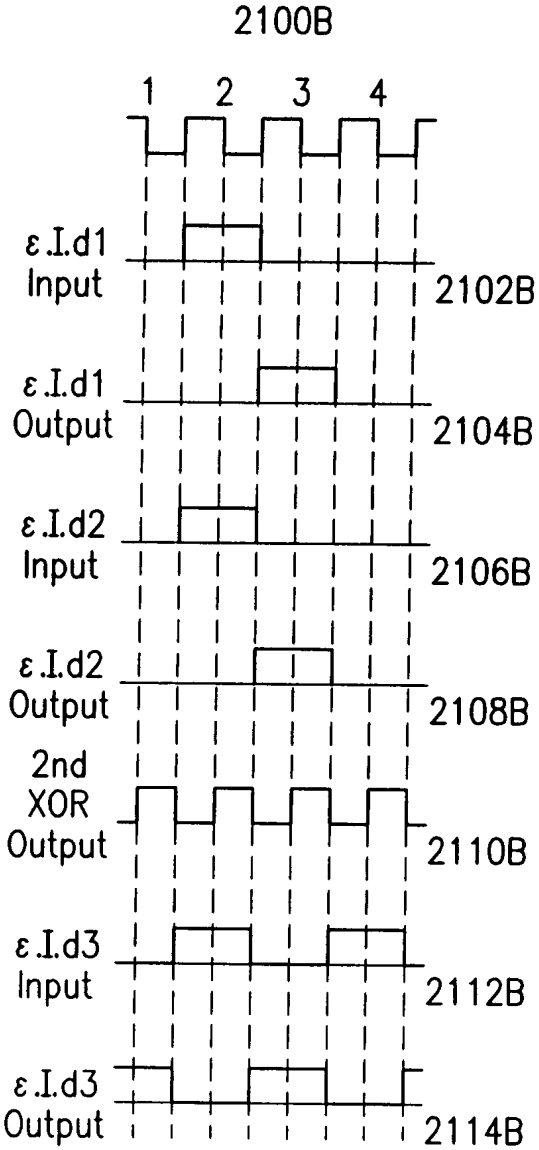

FIG.21B

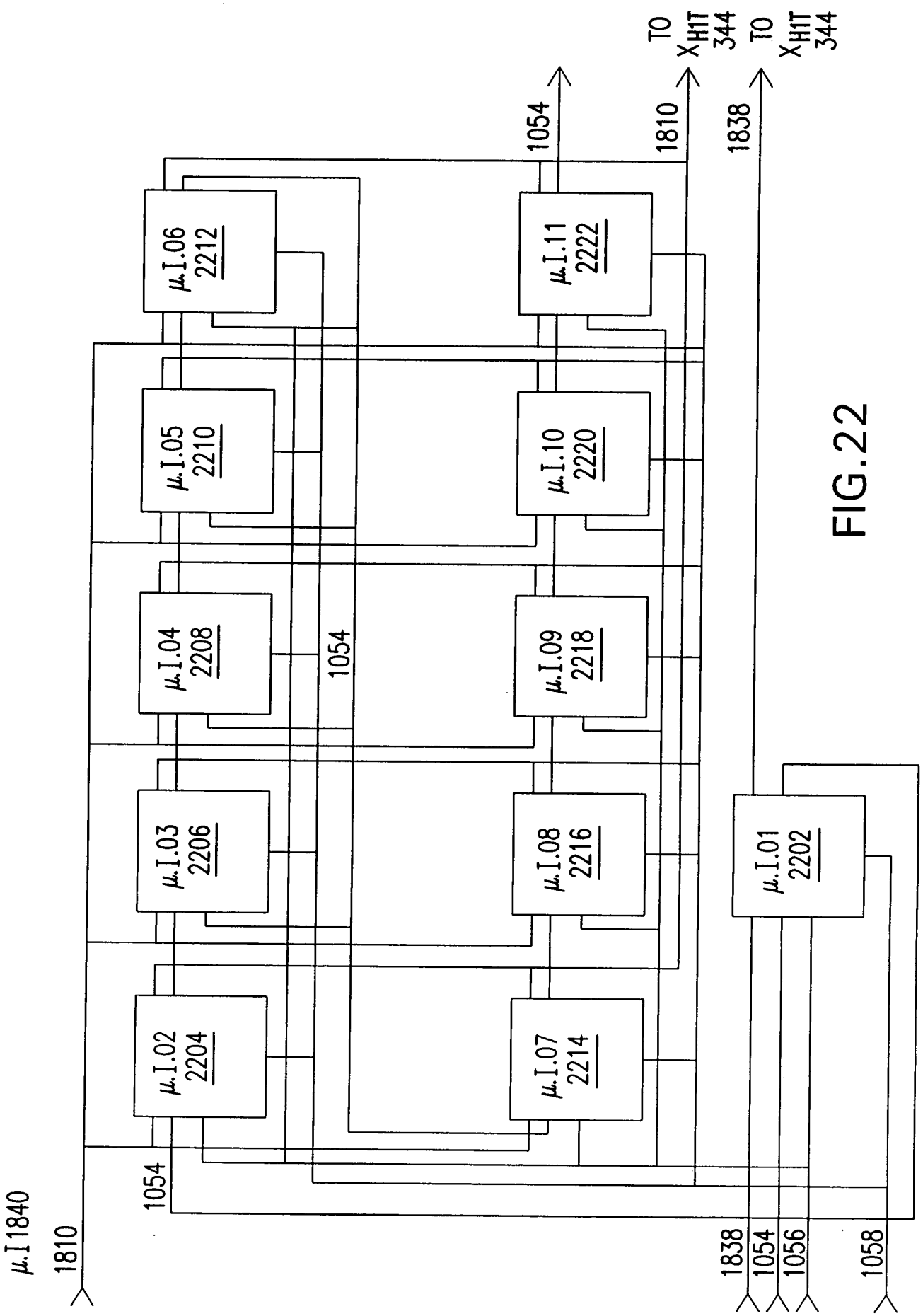
μ.I1840
1810
1054
μ.I.02 2204
μ.I.03 2206
μ.I.04 2208
μ.I.05 2210
μ.I.06 2212
μ.I.07 2214
μ.I.08 2216
μ.I.09 2218
μ.I.10 2220
μ.I.11 2222
μ.I.01 2202
1838
1054
1056
1058
1810
1838
TO X_H1T 344
TO X_H1T 344

FIG. 22

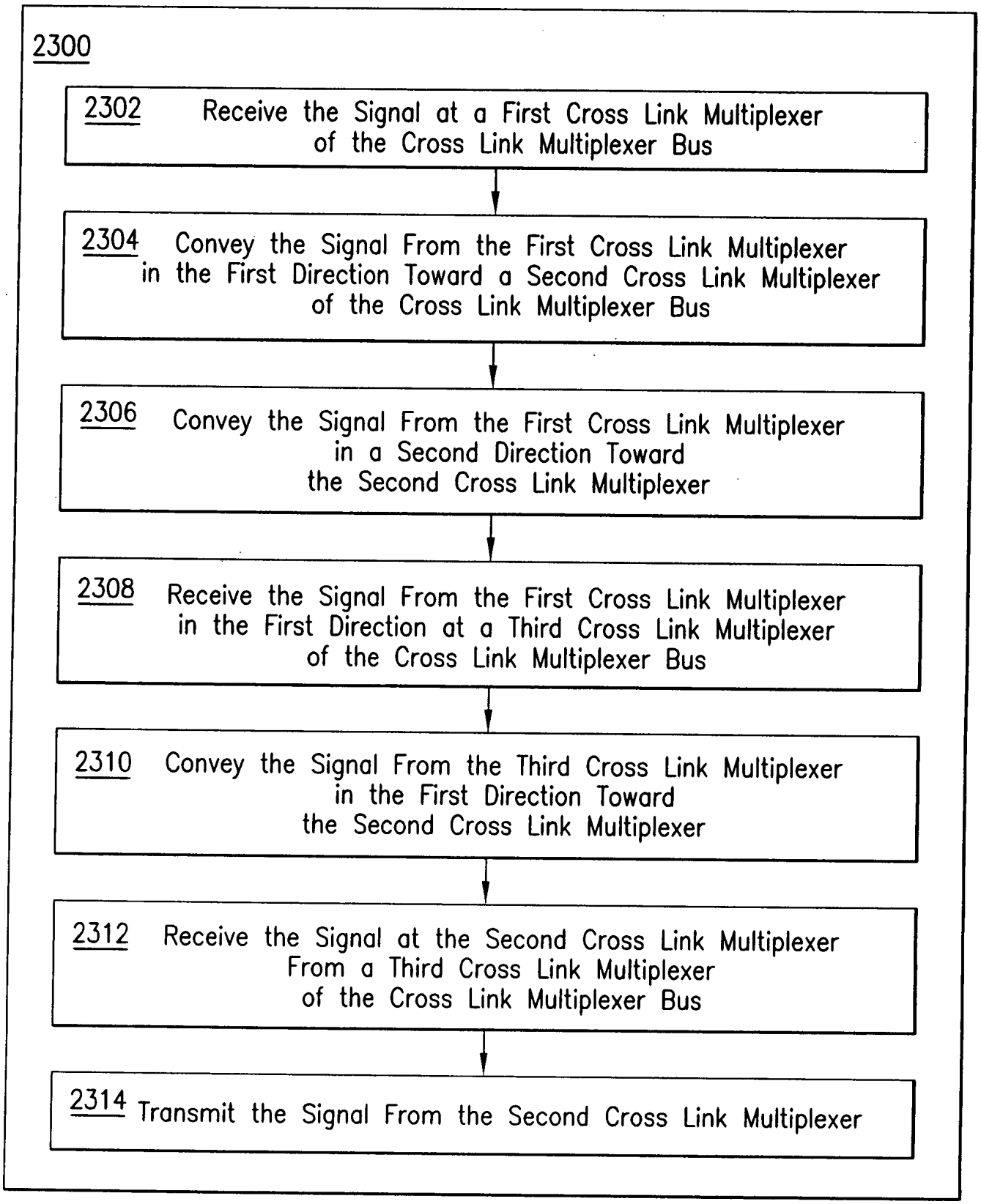
2300
2302 Receive the Signal at a First Cross Link Multiplexer of the Cross Link Multiplexer Bus
2304 Convey the Signal From the First Cross Link Multiplexer in the First Direction Toward a Second Cross Link Multiplexer of the Cross Link Multiplexer Bus
2306 Convey the Signal From the First Cross Link Multiplexer in a Second Direction Toward the Second Cross Link Multiplexer
2308 Receive the Signal From the First Cross Link Multiplexer in the First Direction at a Third Cross Link Multiplexer of the Cross Link Multiplexer Bus
2310 Convey the Signal From the Third Cross Link Multiplexer in the First Direction Toward the Second Cross Link Multiplexer
2312 Receive the Signal at the Second Cross Link Multiplexer From a Third Cross Link Multiplexer of the Cross Link Multiplexer Bus
2314 Transmit the Signal From the Second Cross Link Multiplexer

FIG.23

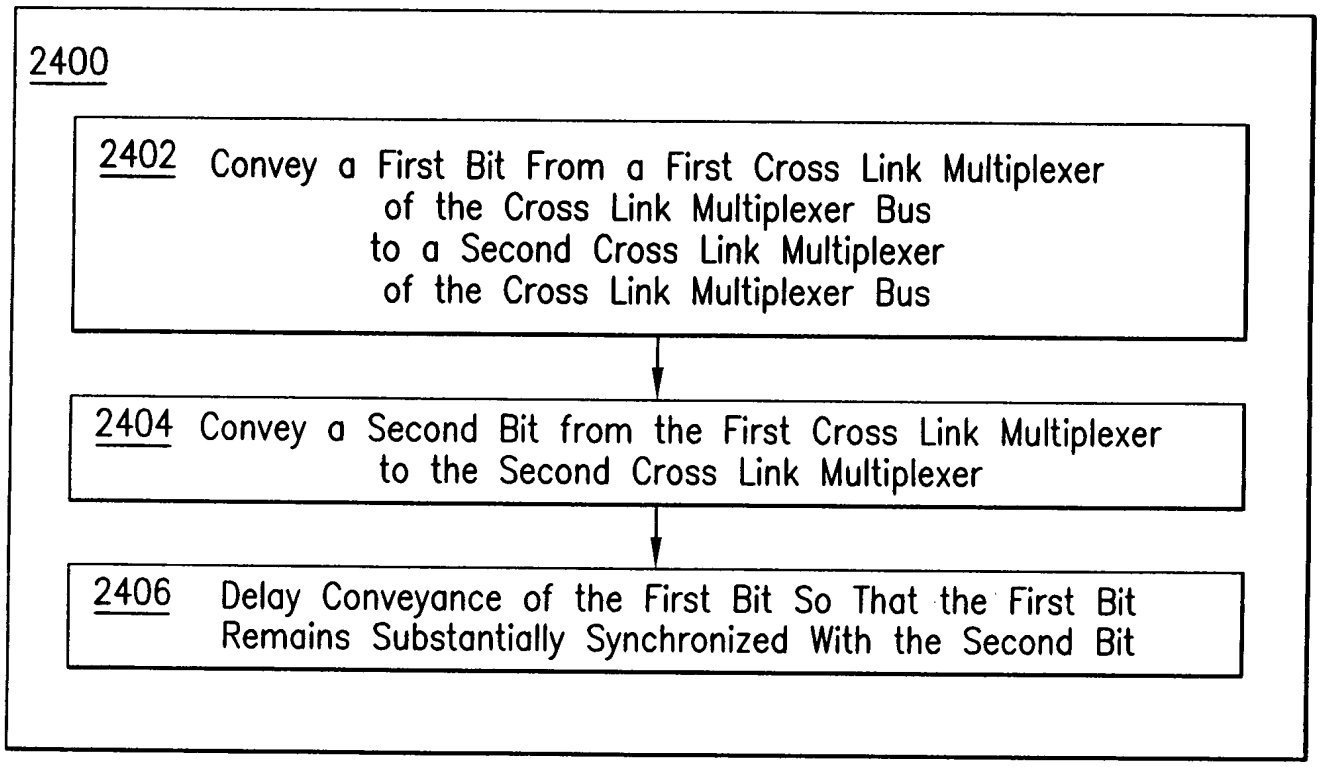
2400
2402 Convey a First Bit From a First Cross Link Multiplexer of the Cross Link Multiplexer Bus to a Second Cross Link Multiplexer of the Cross Link Multiplexer Bus
2404 Convey a Second Bit from the First Cross Link Multiplexer to the Second Cross Link Multiplexer
2406 Delay Conveyance of the First Bit So That the First Bit Remains Substantially Synchronized With the Second Bit

FIG.24

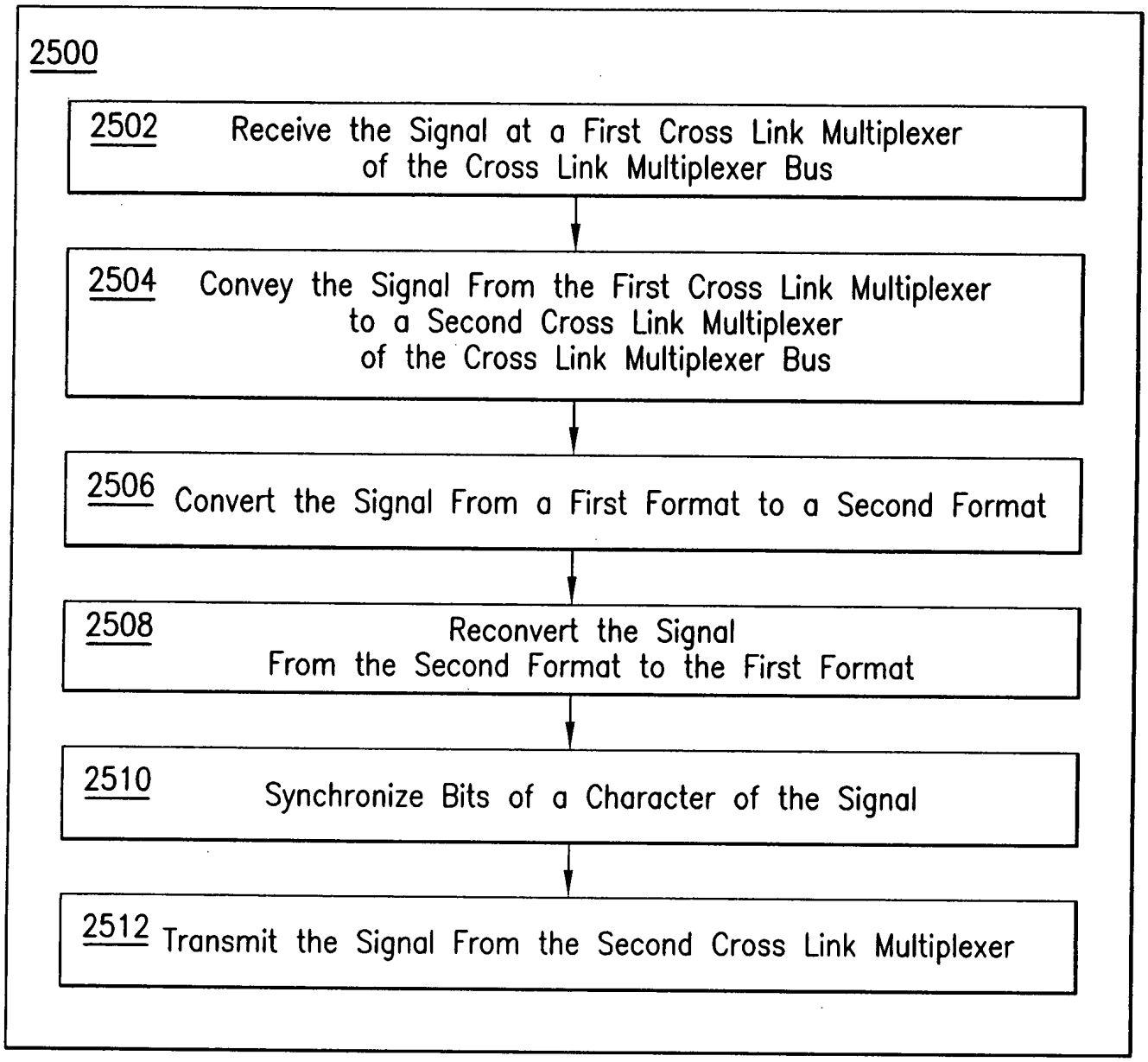
2500
2502
Receive the Signal at a First Cross Link Multiplexer of the Cross Link Multiplexer Bus
2504
Convey the Signal From the First Cross Link Multiplexer to a Second Cross Link Multiplexer of the Cross Link Multiplexer Bus
2506
Convert the Signal From a First Format to a Second Format
2508
Reconvert the Signal From the Second Format to the First Format
2510
Synchronize Bits of a Character of the Signal
2512
Transmit the Signal From the Second Cross Link Multiplexer

FIG.25

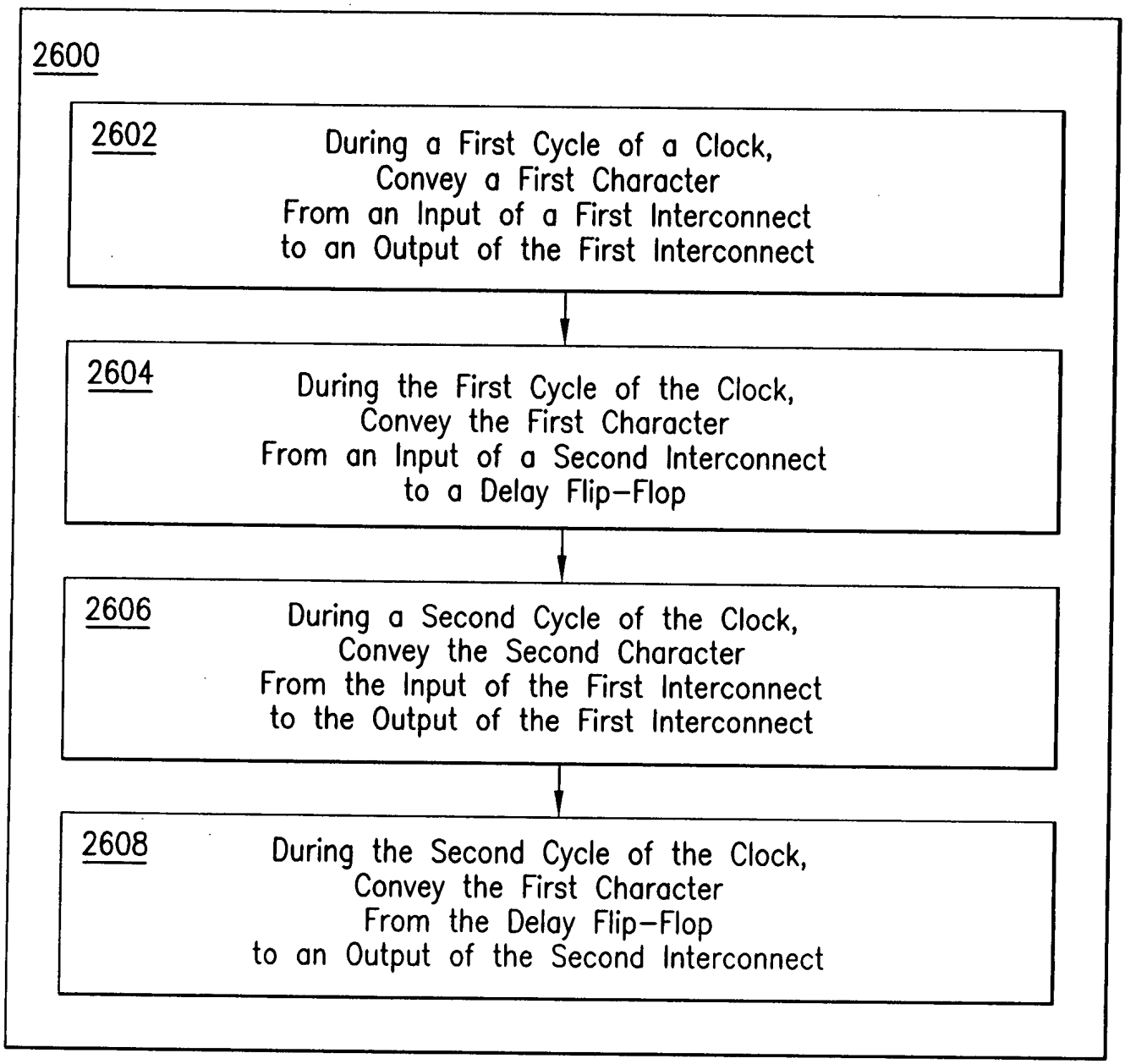
2600
2602
During a First Cycle of a Clock,
Convey a First Character
From an Input of a First Interconnect
to an Output of the First Interconnect
2604
During the First Cycle of the Clock,
Convey the First Character
From an Input of a Second Interconnect
to a Delay Flip-Flop
2606
During a Second Cycle of the Clock,
Convey the Second Character
From the Input of the First Interconnect
to the Output of the First Interconnect
2608
During the Second Cycle of the Clock,
Convey the First Character
From the Delay Flip-Flop
to an Output of the Second Interconnect

FIG.26

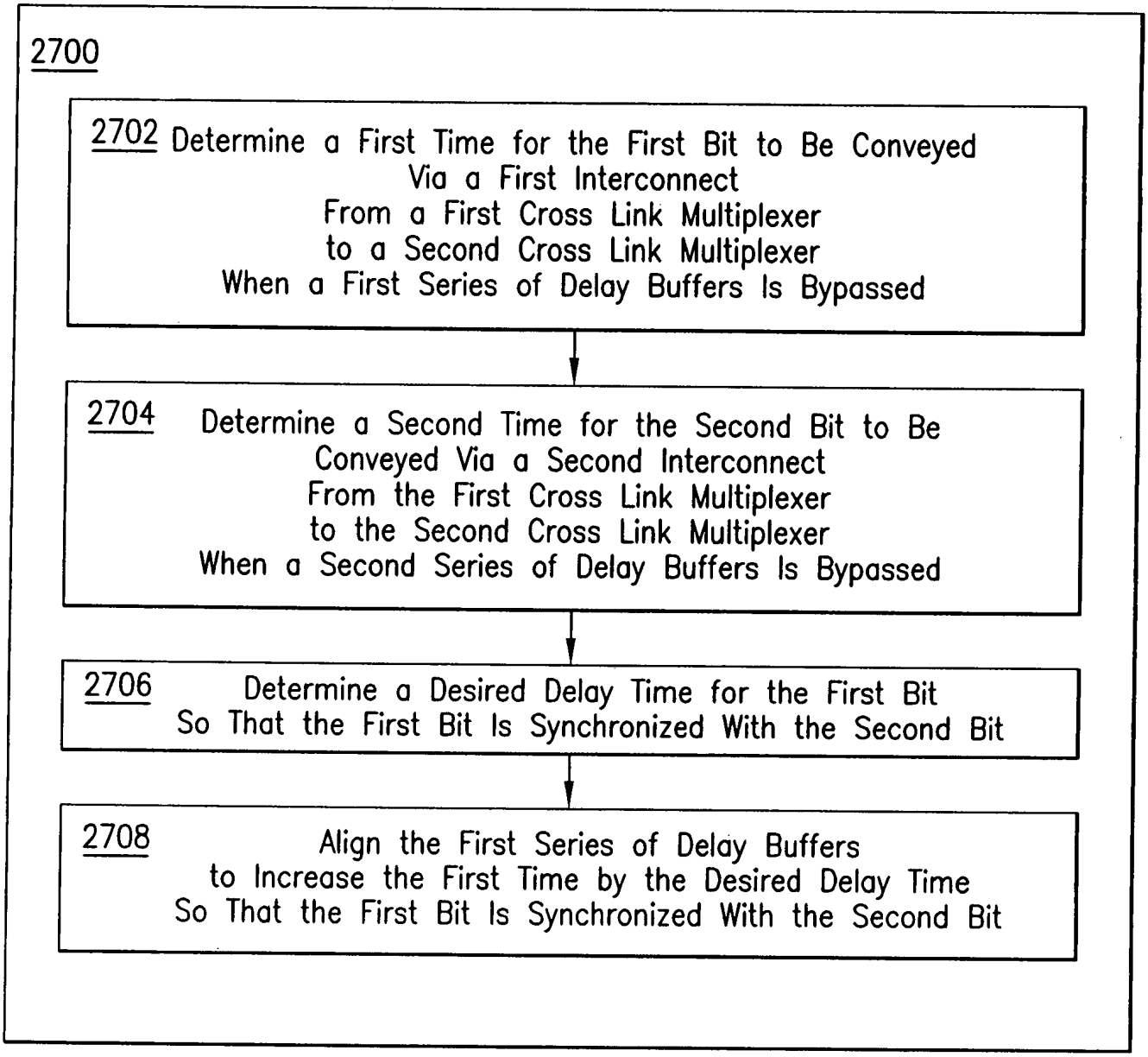
2700
2702 Determine a First Time for the First Bit to Be Conveyed Via a First Interconnect From a First Cross Link Multiplexer to a Second Cross Link Multiplexer When a First Series of Delay Buffers Is Bypassed
2704 Determine a Second Time for the Second Bit to Be Conveyed Via a Second Interconnect From the First Cross Link Multiplexer to the Second Cross Link Multiplexer When a Second Series of Delay Buffers Is Bypassed
2706 Determine a Desired Delay Time for the First Bit So That the First Bit Is Synchronized With the Second Bit
2708 Align the First Series of Delay Buffers to Increase the First Time by the Desired Delay Time So That the First Bit Is Synchronized With the Second Bit

FIG.27

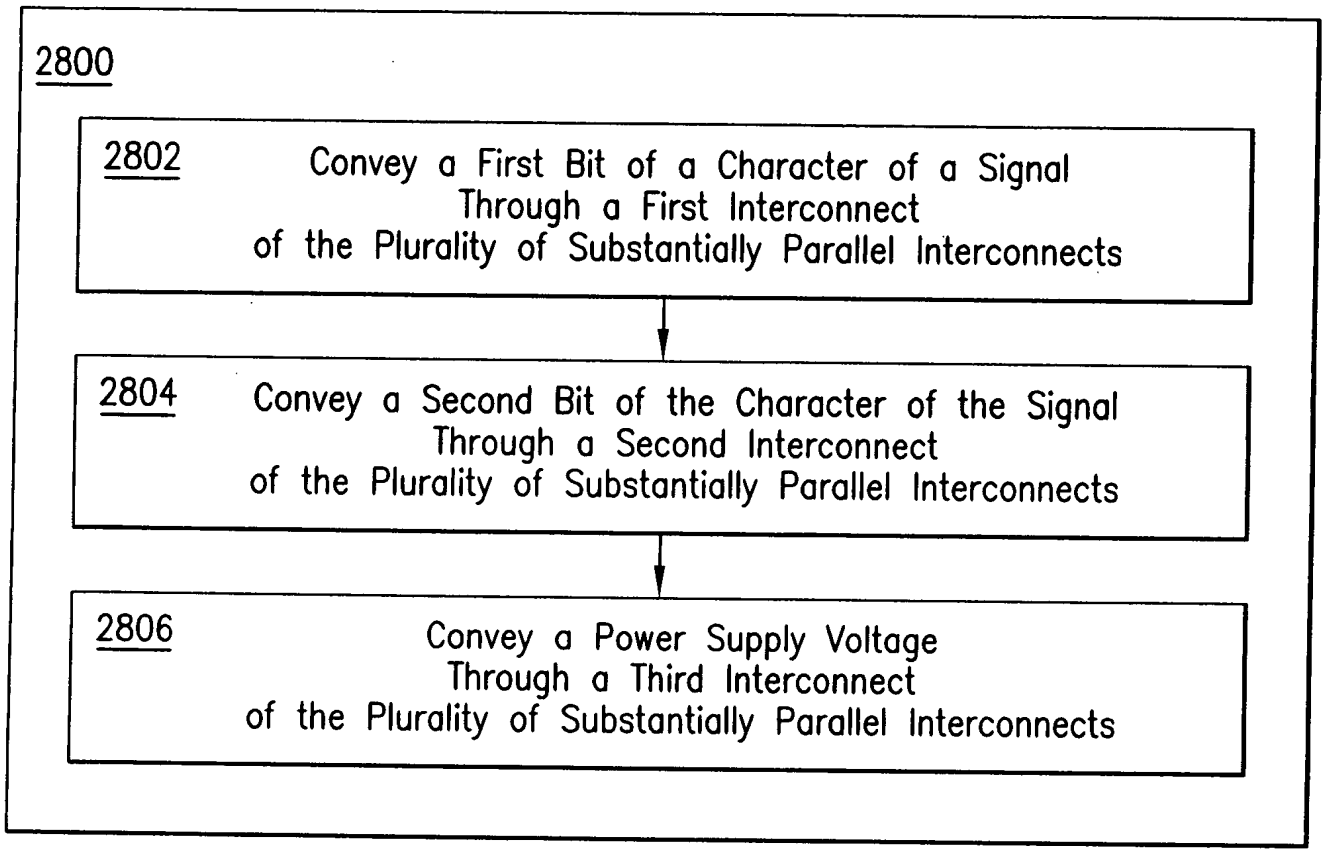
2800
2802
Convey a First Bit of a Character of a Signal Through a First Interconnect of the Plurality of Substantially Parallel Interconnects
2804
Convey a Second Bit of the Character of the Signal Through a Second Interconnect of the Plurality of Substantially Parallel Interconnects
2806
Convey a Power Supply Voltage Through a Third Interconnect of the Plurality of Substantially Parallel Interconnects

FIG.28

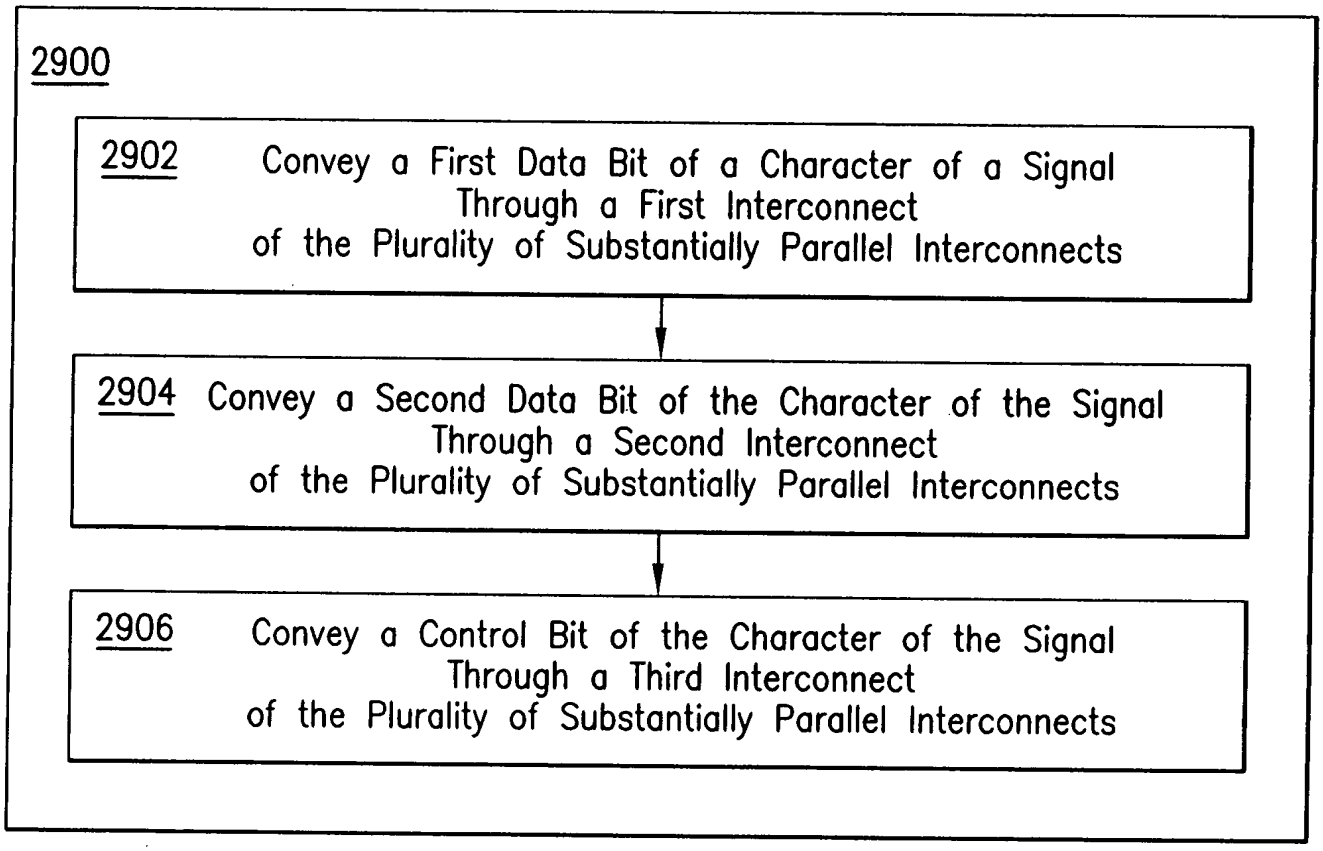
2900
2902
Convey a First Data Bit of a Character of a Signal Through a First Interconnect of the Plurality of Substantially Parallel Interconnects
2904
Convey a Second Data Bit of the Character of the Signal Through a Second Interconnect of the Plurality of Substantially Parallel Interconnects
2906
Convey a Control Bit of the Character of the Signal Through a Third Interconnect of the Plurality of Substantially Parallel Interconnects

FIG.29